CURRENT/VOLTAGE DACS WITH ADCS & DIO ON PCI EXPRESS MINI CARD HARDWARE MANUAL

MODELS **MPCIE-DAAI16-8F, MPCIE-DAAI16-8A, MPCIE-DAAI16-8E**
MPCIE-DAAI12-8F, MPCIE-DAAI12-8A, MPCIE-DAAI12-8E

ACCES I/O Products, Inc.
10623 Roselle Street
San Diego CA 92121-1506 USA

858 550 9559
800 326 1649
sales@accesio.com

www.ACCESIO.COM

MADE IN THE USA

Chapter 1: Quick Start

It is recommended that you install the software package before installing the PCI Express Mini Card (mPCIe) in your computer. You can install the software[1] using a stand-alone installer downloaded from the product page Manuals / Software tab on our website.

Run the installer you downloaded and follow the prompts to install the software for your device.

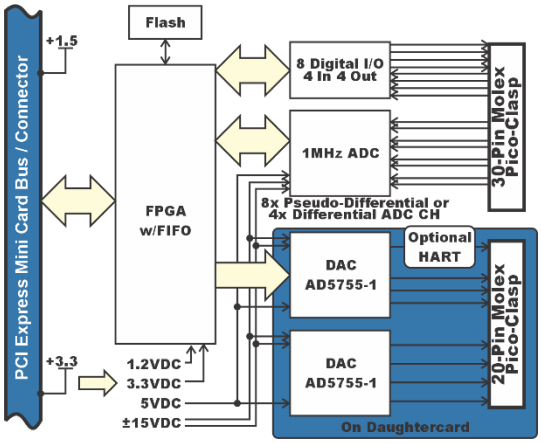
Please note: during the installation you may be prompted regarding the installation of non-WHQL-certified drivers; please carefully confirm the digitally signed source of the drivers and accept the installation.

Once the software has been installed, shut down your system and carefully install the mPCIe card.

Re-start your system. Once the computer finishes booting your new device should already be installed and ready for use; you can confirm this by launching Device Manager and looking under the "Data Acquisition" section. If, for any reason, the mPCIe displays a warning icon, right-click and select "Update Driver".

[1] *In Linux or OSX please refer to github.com/accesio/apci.*

Chapter 2: Introduction

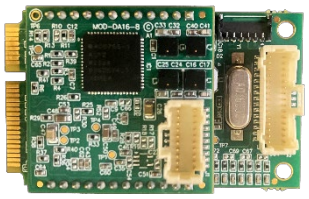


The mPCIe-DAAI16-8F is an ideal solution for adding high-speed analog I/O capabilities to any computer with an mPCIe slot.

FEATURES

- PCI Express Mini Card (mPCIe) type F1, with latching I/O connector (double stack)
- 8× 16-bit DACs capable of Current or Voltage, Waveform streaming at up to 125 ksps, each
  - Software selectable as Voltage or Current output, per channel
  - 0 to 20, 0 to 24, and 4-20mA current output ranges
  - 5V, 10V, ±5V and ±10V voltage output ranges (with optional 20% overrange)
  - Per-Channel offset/scale calibration
- 16-bit, Bipolar, Differential, A/D sampling at up to 1MHz
  - Software selectable as 8 Single Ended or 4 Differential channels
  - 7 channel-by-channel programmable differential input ranges from ±0.3125V up to ±12V
  - High impedance input: 500 MΩ
  - FIFO plus DMA for efficient, robust data streaming
- 8× Digital I/O pins (4 inputs and 4 outputs)
- RoHS compliant standard

The mPCIe-DAAI16-8F is a 16-bit resolution D/A & A/D card with 8 DACs, 8 ADC channels, and 8 DIO. Four DAC voltage ranges (with optional 20% overrange) and 3 current ranges, with both current and voltage outputs, are software selectable.



Each ADC channel can be independently software configured to accept any of 7 input ranges.

This tiny analog I/O card provides the user with everything needed to start acquiring and controlling signals in a variety of applications. The mPCIe-DAAI16-8F data acquisition board can be used in many current real-world applications such as embedded equipment monitoring, precision PC-based and portable environmental measurements, and mobile data acquisition. The card is designed to be used in rugged industrial environments and is a double sided "F1" sized PCI Express Mini Card with a custom daughter-card stacked on top.

A HART (Highway Addressable Remote Transducer) modem option makes this device suitable for a wide array of large-scale infrastructure projects.

Four digital inputs and four digital outputs are provided, with 10kΩ pull-ups on the inputs for contact closure monitoring and 10kΩ pull-downs on the digital outputs to avoid spurious control signals on power-up or reset.

Applications: Optical Networking, Instrumentation, Multichannel Data Acquisition and system monitoring, Automatic Test Equipment, Process Control and Industrial Automation, Power line monitoring.

Chapter 3: Hardware

This manual applies to the following models:	
mPCIe-DAAI16-8F	mPCIe, 8 16-bit D/A with 8 A/D at up to 1 msps
mPCIe-DAAI16-8A	mPCIe, 8 16-bit D/A with 8 A/D at up to 500 ksps
mPCIe-DAAI16-8E	mPCIe, 8 16-bit D/A with 8 A/D at up to 250 ksps
mPCIe-DAAI12-8A	mPCIe, 8 16-bit D/A with 8 12-bit A/D at up to 500 ksps
mPCIe-DAAI12-8	mPCIe, 8 16-bit D/A with 8 12-bit A/D at up to 250 ksps
mPCIe-DAAI12-8E	mPCIe, 8 16-bit D/A with 8 12-bit A/D at up to 100 ksps

These models are full-length "F1" mPCIe devices (30 × 50.95 mm) in a double-stack configuration and include 9" (229mm) 20-conductor cable to DB-25F pin and a 30-conductor cable to a DB-37F. All units are RoHS compliant.

INCLUDED IN YOUR PACKAGE

9" 20-pin cable (228mm)
9" 30-pin cable (228mm)
DAC/ADC/DIO mPCIe card (double stack)

Available accessories include:	
ADAP37M-MINI	37-pin Direct Connect Terminal Board
ADAP25M	25-pin Direct Connect Terminal Board
mPCIe-HDW-KIT2	Mounting hardware for 2mm
mPCIe-HDW-KIT2.5	Mounting hardware for 2.5mm

Contact the factory for information regarding additional accessories, options, and specials that may be available to best fit your specific application requirements, such as extended temperature, conformal coating, or alternate cable lengths, to name a few.

Chapter 4: Configuration Settings

There are no configuration options to set. Contact the factory for customization options.

Chapter 5: PC Interface

This product interfaces with a PC using a PCI Express Mini Card (mPCIe) connection; a small-form-factor, high-performance, rugged peripheral interconnect technology first introduced for use in laptops and other portable computers.

mPCIe's small size and powerful performance, combined with perfect software compatibility with PCI and PCIe peripheral designs, have led to its recent adoption as a go-to standard for embedded Data Acquisition and Control, and many other applications.

Although mPCIe is a broadly-adopted industry standard, the actual connection to the computer shares a specification with mSATA: both mSATA and mPCIe use the same edge-connector. In fact, well-designed PCs can automatically detect and configure their onboard connectors to work with either mPCIe or mSATA devices – and, according to the standards for mPCIe and mSATA they are *supposed* to do so! However, some PC manufacturers ship computers that *only* support mSATA devices. Please confirm in your PC documentation that your edge-connector is *actually* PCI Express Mini Card compliant before installing this, or any, mPCIe card. Damage might occur if you install an mPCIe device into a computer that only supports mSATA.

mPCIe defines mounting holes for securing the otherwise loose end of the card, so it is impossible for these cards to wiggle or flap themselves loose (which was a recurring problem with the older PCI Mini devices). Eliminating this concern for PCI Express Mini Cards is a major reason this standard has seen rapid adoption by the Data Acquisition and Control industry.

The mPCIe standard, like its PCI Mini Card predecessor, was designed assuming use primarily in Laptop or Notebook and similar devices, where physical dimension is often the paramount design constraint. In Data Acquisition and Control applications low-weight combined with vibration tolerance tend to be of more concern.

Chapter 6: I/O Interface

Custom hardware interfaces can be produced to fit your specific application requirement.

All DAC outputs, both current mode and voltage, are provided on the 20-pin header located on the top board of the double-stack. This is normally used with the 9" 20-pin to DB-25 cable for all analog output connections.

All ADC channels and DIO pins are provided on the 30-pin header located on the base board of the double-stack. This is normally used with the 9" 30-pin to DB37 cable for all analog input and digital I/O connections.

DB-25F Female Pinout DAC			
1	DAC 0		
2	GND	14	GND
3	DAC 1	15	DAC 7
4	GND	16	GND
5	DAC 2	17	GND
6	GND	18	GND
7	DAC 3	19	GND
8	GND	20	NC
9	DAC 4	21	NC
10	GND	22	NC
11	DAC 5	23	NC
12	GND	24	NC
13	DAC 6	25	NC

Molex 20-pin Pinout DAC			
1	DAC 0	2	GND
3	DAC 1	4	GND
5	DAC 2	6	GND
7	DAC 3	8	GND
9	DAC 4	10	GND
11	DAC 5	12	GND
13	DAC 6	14	GND
15	DAC 7	16	GND
17	GND	18	GND
19	GND	20	GND

DB-37F Female Pinout ADC/DIO			
1	ADC 0		
2	ADC 1	20	NC
3	ADC 2	21	NC
4	ADC 3	22	NC
5	GND	23	NC
6	ADC 4	24	NC
7	ADC 5	25	NC
8	ADC 6	26	NC
9	ADC 7	27	NC
10	GND	28	DGND
11	COMMON	29	DO 0
12	GND	30	DO 1
13	GND	31	DO 2
14	GND	32	DO 3
15	GND	33	DGND
16	USER VCC	34	DI 0
17	GND	35	DI 1
18	GND	36	DI 2
19	GND	37	DI 3

Molex 30-pin Pinout ADC/DIO			
1	ADC 0	2	ADC 4
3	ADC 1	4	ADC 5
5	GND	6	GND
7	ADC 2	8	ADC 6
9	ADC 3	10	ADC 7
11	GND	12	GND
13	COMMON	14	GND
15	GND	16	GND
17	USER VCC	18	GND
19	GND	20	DO 0
21	DO 1	22	DO 2
23	DO 3	24	DI 0
25	DI 1	26	DI 2
27	DI 3	28	DGND
29	DGND	30	DGND

Chapter 7: Software Interface

How to use

The ADC used, the ADAS3022, is a flexible data acquisition system-on-chip that has numerous features and modes of operation, and additional modes and features are added by our advanced FPGA design.

This flexibility can seem overwhelming, but we've designed our AIOAIO.dll API to make using this ADC simple for 99% of customer use-cases, based on 30+ years of customer feedback.

We strongly recommend you ignore the register details provided in Chapter 7: Software Interface and the discussions regarding low-level control of the ADC in the second half of this chapter. Instead, simply refer to the AIOAIO Software Reference (.html) manual [link] and the source code to the variety of sample programs provided in the Software Installation Package [link].

Tip: Taking data from every channel can be as simple as calling "ADC_GetImmediateScanV(0, rangeCode, &data);", which converts all channels at the specified range and stuffs the data (as double-precision floating point Voltages) into the data array. This function can be called many thousands of times per second. Please refer to the samples and the software reference for details on this and other available API functions, including how to acquire 1MHz data via callback or polling.

Advanced Topics

BASIC, ADVANCED, AND NON-SEQUENCED MODES

The ADAS3022 uses the SEQ1:0 bits in the +38 control register to select between non-sequenced mode, basic sequence mode, and advanced sequence mode.

SEQ1	SEQ0	Mode	Description
0	0	non-Sequenced	The ADAS will acquire data from the channel specified in the INx2:0 bits, at the gain specified in the Gain2:0 bits.
0	1	Modify Basic Sequence	Allows the gain and such to be modified while running a basic sequence, without starting conversions over at CH0.
1	0	Advanced Sequence	Acquires Channel 0 using the gain selected via +18 bits 2:0. Conversion-starts will automatically cycle through the channels from CH0 through INx2:0, and each channel is acquired at the per-channel gain set in +18. The sequence repeats, starting at CH0 after INx2:0 is acquired.
1	1	Basic Sequence	Acquires channel 0 using the gain set in Gain2:0. Conversion-starts will automatically cycle through the channels from CH0 through INx2:0, but all channels are acquired using the gain set in Gain2:0 rather than using the gains from +18. The sequence repeats, starting at CH0 after INx2:0 is acquired.

SOFTWARE, PERIODIC, AND EXTERNAL START ADC CONVERSION TIMING MODES

ADC data can be acquired periodically, synchronous to an external digital input, or asynchronously via software command.

Single, Asynchronous: If the +10 ADC Timing divisor is zero then writing to +38 with bit 16 set (to 1) will initiate a single ADC Start Event under software control.

Periodic, Asynchronous: If the +10 ADC Timing divisor is non-zero, and the External ADC Trigger Digital Input Secondary function is *not* enabled, writing to +38 with bit 16 set will initiate a single ADC Start Event, and subsequent events will occur at the rate selected via +10's divisor. This is "software initiated periodic timed ADC" data.

External Trigger, Periodic, Synchronous: If the +10 ADC Timing divisor is non-zero, and the External ADC Trigger Digital Input Secondary function *is* enabled, writing to +38 with bit 16 set *ARMS* the card to begin the periodic collection of ADC data. No data will be collected until the selected edge occurs on the ADC Trigger input. (Refer to +44 for additional details on the Digital I/O Secondary Functions.) Once triggered, data will be collected until manually stopped by writing +38 with bit 16 clear (or various resets, etc.).

External Start, Single, Synchronous: The digital input secondary function "ADC Start" can be configured to initiate individual ADC Start Events on a selected edge input.

SINGLE AND SCAN START MODES

Each ADC Start Event can be configured to start either a Scan of channels or a single channel conversion.

Single Start Mode: Writing to +38 with bit 18 clear (to 0) selects "Single Start Mode". Each ADC Start Event, regardless of source, will acquire one channel. No subsequent conversions will occur until the next ADC Start Event.

Scan Start Mode: Writing to +38 with bit 18 set (to 1) selects "Scan Start Mode". Each ADC Start Event will acquire the full configured sequence of channels, starting with CH0 and proceeding through INx2:0, then no further data will be acquired until a subsequent ADC Start Event. The channels within this "scan" of data are acquired at the rate selected via +14. Bit 18 is ignored (assumed zero) if non-Sequenced mode is set (SEQ1:0=00) or if INx2:0==0.

Software Pro Tips:

- Use our API. Avoid accessing the card registers unless you really know you need to. Contact us for any questions, we're here to help.
- Always use Advanced Sequencer Mode.
- Always use Scan Start Mode.
- Set the periodic rate at +10, set the inside-scan channel rate at +14, configure External Trigger if you are using it, configure the per-channel gains at +18, then write to +38 to Start or Arm (in Software or ADC Trigger modes, respectively) the Periodic Scans.

Register Overview

Register Offset [hex]	Read /Write	Register Name	Register Description Note: All registers must be accessed as 32-bits
+0	R/W	Resets and Power	Board and Feature Reset command bits and ADC Power-Down control bit and status
+4	W	DAC Control	DAC (LTC2664) Command Register bits
+8	W	DAC Waveform Divisor	DAC Waveform Points/second, divisor = 25 MHz / DAC Waveform Rate
+C	R	ADC Base Clock	Frequency of the ADC Sequencer Base Clock (Hz) used to calculate the ADC Rate Divisor for desired conversion rates
+10	W/R	ADC Rate Divisor	ADC Start Rate = ADC Base Clock / ADC Rate Divisor (this register)
+14	W/R	ADC Rate Divisor #2	Controls rate of channels inside each scan when running in scan-start mode
+18	W/R	ADC ADV Sequence Gain	Each nybble controls the gain code (input range) of the respective ADC channel
+20	W/R	ADC FAF Threshold	ADC FIFO Almost Full Threshold, can be enabled to generate IRQs when the threshold amount of ADC data is available in the FIFO
+28	R	ADC FIFO Count	ADC FIFO Depth: read to determine how much data is available in the FIFO
+30	R	ADC FIFO Data	ADC FIFO
+38	W/R	ADC Control	ADAS3022 and ADC Control bits
+40	W/R	IRQ Enable / Status	IRQ Latch Clear bits and IRQ Enable Control bits ÷ IRQ Latch Status and IRQ Enable Status
+44	W/R	DIO Data	16-bits of DIO Data. Must be read/written as a 32-bit DWORD value
+48	W/R	DIO Control	Digital Secondary Function enable bits and direction control for a total of nine I/O Groups (DIO 15, 14, 13, 12, 11, 10, 9, 8, and 7:0)
+50	RW	DAC Waveform FIFO	Write DAC Control values here to load into the DAC Waveform FIFO; read to determine how many samples are in the FIFO
+54	W	DAC Waveform DACs/Point	Write 1, 2, 3, or 4 to configure how many samples are written from the DAC Waveform FIFO to the DACs on each DAC Waveform tick
+58	R	DAC Waveform FIFO Size	Size of the DAC Waveform FIFO (+50) in number of 32-bit DAC control values (0x2000 is typical)
+68	R	Revision	FPGA code revision

All of these registers can be operated from any operating system using any programming language, using either no driver at all (kernel mode, Linux ioperm(3), DOS, etc.) or using one of the ACCES provided drivers (AIOWDM [for Windows], APCI [for Linux & OSX]), or using any 3rd party APIs such as provided with Real-Time OSes. Addresses not explicitly documented are factory reserved and should not be accessed.

REGISTER DETAILS

Register bits labeled UNUSED or RSV are reserved and should be cleared to zero in all write operations and ignored in all read operations.

Resets and Power, Offset +0 of 64-bit Memory BAR[2+3] Read/Write 32-bits only

bit	D31 THROUGH D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	UNUSED	RST HART	DAC4-7 CLEAR	DAC0-3 CLEAR	RST DAC FIFO	RST ADC FIFO	RST DIO	RST DAC4-7	RST DAC0-3	PD ADC	RST ADC	RST BOARD

RST HART: Write 1 to bit D10 to reset the (optional) HART modem.
DAC4-7 CLEAR: Write 1 to bit D9 to clear DACs0-3 to their pre-programmed clear code. Consult the AD5755-01 datasheet for more information.
DAC0-3 CLEAR: Write 1 to bit D8 to clear DACs0-3 to their pre-programmed clear code. Consult the AD5755-01 datasheet for more information.
RST DAC FIFO: Writing with bit D7 set will reset the DAC Waveform FIFO, making it empty
RST ADC FIFO: Writing with bit D6 set will reset the ADC FIFO, returning it to the power-on / reset state: emptying the FIFO by throwing away the contents.
RST DIO: Writing with bit D5 set will reset the Digital I/O circuits to their power-on / reset state: returning all I/O Groups to input mode and disabling secondary functions.
RST DAC: Writing with bit D3 set will reset the Analog Output circuits to their power-on / reset state: ±10V range on all DAC outputs with 0V on each output.
PD ADC: Writing a 1 will power the ADAS3022 down. Write a 0 to power the ADAS3022 back up. Only this bit does not auto-clear to zero on write.
RST ADC: Writing a 1 will reset the Analog Input circuits to their power-on / reset state: see each ADC Register for more details
RST BOARD: Writing a 1 will reset the entire device to its power-on / reset state.

All RST and CLEAR bits are "command" bits: a 1 causes the reset to occur, and the bit is automatically cleared by the FPGA.

DAC Control, Offset +4 of 32-bit Memory BAR[1] Read/Write 32-bits only

bit	D31	D30	D29	D28	D27-D24	D23 through D0
Name	DAC SPI busy	LDAC	DAC FIFO EMPTY	DAC FIFO HALF	unused	AD5755-01 DAC Control Bits

Bits 31, 30, 29, and 28 are read-only.
Bit 31: If set the DAC SPI bus is busy; avoid writing to +4 while this bit is set
Bit 30: Set each time the LDAC signal is issued to the DAC IC, and cleared by reading this register (+4)
Bit 29: If set the DAC Waveform FIFO is empty
Bit 28: If set the DAC Waveform FIFO is less than half full
Please refer to the AD5755-01 Data Sheet for details regarding bits D23-D0. Note: PEC Mode is not supported.
Consult the AIOAIO Software Reference, or our sample programs' source, to avoid the hassle:

```
DAC_SetRange1(iBoard, iChannel, iRange);
DAC_OutputV(iBoard, iChannel, double Voltage);
```

DAC Waveform Rate Divisor, Offset +8 of 32-bit Memory BAR[1] Read/Write 32-bits only

Write a 32-bit divisor to control the speed at which DAC Waveform playback occurs (Points per second). Each timeout of this clock causes the DACs to simultaneously output the last loaded values; the FPGA then writes the next Point from the DAC Waveform FIFO to the DAC chip. A Point consists of 1, 2, 3, up to 8, DAC control words as specified at +54.

DAC Waveform Rate Divisor = integer(25000000 ÷ Target DAC Waveform Output Rate)
Actual DAC Waveform playback (Points/second) Rate (Hz) = Base Clock ÷ DAC Waveform Rate Divisor

Base Clock, Offset +C of 32-bit Memory BAR[1] Read Only 32-bits only

Base Clock: Reading this 32-bit register returns the speed (in Hertz) of the clock used to generate ADC Start Conversions. Typical value is 50Million (50 MHz), but for broadest compatibility software should always read this register during init, and always use the read value when calculating what, if any, divisors to write to the ADC Rate Divisor and Watchdog timeout registers. Note: The DAC Waveform clock uses 25 MHz, not 50 MHz.

ADC Base Clock, Offset +C of 64-bit Memory BAR[2+3] Read Only 32-bits only

ADC Base Clock: Reading this 32-bit register returns the speed (in Hertz) of the clock used to generate ADC Start Conversions. Typical value is 50 Million (50MHz), but for broadest compatibility software should always read this register during init, and always use the read value when calculating what, if any, divisor to write to the ADC Rate Divisor register.

ADC Rate Divisor, Offset +10 of 64-bit Memory BAR[2+3] Read/Write 32-bits only

ADC Rate Divisor: Write a 32-bit divisor to the ADC Rate Divisor register to control the speed at which ADC Start events occur.

Actual ADC Start Rate (Hz) = ADC Base Clock ÷ ADC Rate Divisor
ADC Rate Divisor = integer(ADC Base Clock ÷ Target ADC Start Rate)

In ADC Scan Start mode each timeout of the +10 divisor begins a scan of channels. In all other modes the +10 rate selects the conversion rate per-channel.

ADC Rate Divisor #2, Offset +14 of 64-bit Memory BAR[2+3] Read/Write 32-bits only

ADC Rate Divisor #2: Write a 32-bit divisor to the ADC Rate Divisor #2 register to control the speed at which ADC Conversions occur within each scan when running in ADC Scan Start Modes.

In "ADC Scan" start modes only, one Scan of ADC CH0 through the channel selected in +38 INx2:0 bits occurs at the rate selected at +10. During each Scan the first channel is converted immediately, and subsequent channels are acquired at the rate selected at +14.

ADC Advanced Sequencer Gain Control, Offset +18 of 64-bit Memory BAR[2+3] Read/Write 32-bits only

bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RSV	AIN 7 GAIN2:0			RSV	AIN 6 GAIN2:0			RSV	AIN 5 GAIN2:0			RSV	AIN 4 GAIN2:0			RSV	AIN 3 GAIN2:0			RSV	AIN 2 GAIN2:0			RSV	AIN 1 GAIN2:0			RSV	AIN 0 GAIN2:0		

Each nybble configures the gain of the corresponding Analog Input channel ONLY when the ADC is running in Advanced Sequenced mode.

Table 1 - Gain Codes

GAIN2:0 "gain code"	D2	D1	D0	Range Volts *per pin*[1]	Range V p-p, MAX[1]	µV/Count	Differential rejection V	Notes
0	0	0	0	±12	49.15	750		The voltage range is shown as recommended max voltage per input pin. The recommendation is slightly narrower than max to allow calibration. The voltages that can be *measured,* between the + input and the – or COMMON inputs, are double: the ±12V range will return voltages between +24V and -24V, or "48V p-p".
1	0	0	1	±5	20.48	312.5	±5.12	
2	0	1	0	±2.5	10.24	156.3	±7.68	
3	0	1	1	±1.25	5.12	75.13	±8.96	
4	1	0	0	±0.625	2.56	39.06	±9.60	
5	1	0	1	±0.3125	1.28	19.53	±9.92	
7	1	1	1	±10	40.96	625		

Gain code 6 (110) is reserved and will result in undefined behavior

Note 1: Applying +V to IN+ and -V to IN- (or ADC COMMON) results in 2×V span; reversing the voltage polarity results in another 2×V span, for a total Peak-to-Peak measurement capability of 4×V p-p

ADC FIFO Almost Full IRQ Threshold, Offset +20 of 64-bit Memory BAR[2+3] Read/Write 32-bits only

bit	D31 through D12	D11 through D0
Name	UNUSED	FAF

FAF: Write any 12-bit value (0..4095) to set the amount of entries in the ADC FIFO allowed to accumulate before a FIFO Almost Full IRQ is fired.
In Software ADC Start mode (ADC Rate Divisor (+10) cleared to zero) the FIFO is 32-bits wide, able to hold up to 4095 conversion results (+statuses).
In all other ADC Start Modes the ADC FIFO is 64-bits wide, holds two ADC Conversions (+statuses) per FIFO entry and the FIFO thus holds 8190 conversion/status pairs. Refer to the ADC FIFO (+30) register description for more details.

ADC FIFO Count, Offset +28 of 64-bit Memory BAR[2+3] Read-Only 32-bits only		
bit	D31 through D12	D11 through D0
Name	UNUSED	FIFO Count

FIFO Count: Read FIFO Count to determine how many entries the ADC FIFO contains.
In Software ADC Start Mode (ADC Rate Divisor (+10) cleared to zero) the FIFO Count determines how many ADC Conversions (+statuses) are held in the FIFO. Read the ADC FIFO this many times to gather the acquired ADC Data.
In all other modes the FIFO Count reports the number of *pairs* of ADC Conversions are available in the FIFO. Were you to read the data from the ADC FIFO (+30) you would read two 32-bit values per FIFO Count to gather the acquired data. However, in these modes it is generally best to let DMA transfer the FIFO data, which is performed at the native 64-bit FIFO width.

ADC FIFO Data, Offset +30 of 64-bit Memory BAR[2+3] Read-Only 32-bits only													
bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22 through D20	D19	D18 through D16	D15 through D0
Name	INVALID	RUNNING	DIO3	DIO2	DIO1	DIO0	TEMP	MUX	RSV	Channel	Diff	Gain	ADC Counts (Two's complement)

ADC FIFO Data: Read the RAW-format ADC Conversion results (in twos-complement 16-bit form) and the associated status word.

INVALID: If INVALID is SET then all other bits are undefined and the entry should be discarded. This can occur if you read from the ADC FIFO while the ADC FIFO Count (+28) is zero.

RUNNING: SET indicates the ADC Sequencer is operating, taking either periodic (timer-driven) conversions or via the external ADC Start secondary digital function.

DIO3:0: These four bits indicate the state of the corresponding digital I/O pin at the time the paired ADC Conversion was sampled.

TEMP: If TEMP is SET the ADC Counts are acquired from the ADAS3022's onboard temperature sensor rather than from an analog input channel. Refer to ADC Control (+38) for more information about acquiring the temperature data.

MUX: If MUX is SET the ADC Counts are acquired from the ADAS3022's Auxiliary Mux inputs rather than from the normal Analog Input Channels. Note, the mPCIe-ADIO16-8F does not have anything usefully connected to the Aux Mux inputs and you should not bother acquiring data from them.

Channel2:0: The 3 Channel bits indicate from which Analog Input the paired ADC Counts were sampled. Refer to ADC Control (+38) for important information about the Channel bits re Differential operation.

Diff: SET indicates the paired ADC Counts were sampled in Differential mode. Refer to ADC Control (+38) for important information about the Channel bits re Differential operation.

Gain2:0: The 3 Gain bits indicate at what gain code the paired ADC Counts were sampled. Refer to the gain code table in ADC Advanced Sequencer Gain Control (+18) for how to interpret the Gain bits.

ADC Counts: 16-bit two's complement ADC counts, the ADC conversion result from the samples Channel at the specified Gain, sampled in Differential or Singled-ended / Pseudo-Differential mode as indicated by the Diff bit (D19).

Please refer to the sample program's source for details on how to translate RAW-format ADC data into Volts — or skip the hassle and use our AIOAIO.dll API Library:

ADC_GetImmediateV(iBoard, pVolts, iChannel, iRange);, ADC_GetImmediateScanV(iBoard, pVolts[]); etc.

ADC Control, Offset +38 of 64-bit Memory BAR[2+3] Read/Write 32-bits only															
bit	D31 through D19	D18	D17	D16	D15	D14 through D12	D11	D10	D9 through D7	D6	D5 through D4	D3	D2	D1	D0
Name	UNUSED	SCAN	CONFIG	GO	RSV	INx2:0	COM	RSV	Gain2:0	/MUX	SEQ1:0	/TEMP	RSV	CMS	RSV

The ADAS3022 is a very flexible ADC module and we highly recommend you use the AIOAIO.dll-provided API to avoid needing to know the following information.

SCAN: If SCAN is set (to 1) *AND* INx2:0 is non-zero then each "ADC Start" event will acquire channels 0 through INx2:0 at the rate specified in +14.

CONFIG: If CONFIG is set then the ADC control bits (D15 through D0 of this register) will be written to the ADAS3022

GO: If GO is set then, if +10 is non-zero the card will begin taking ADC conversions or scans at the rate set via +10; if +10 is zero then a single ADC conversion or scan will be taken.

INx2:0: INx specifies the individual channel to convert (in non-sequenced modes) or the last channel of the 0-INx sequence to be converted.

COM: If COM is set then each conversion will be the measurement between the IN+ pin and COMMON (single-ended or pseudo-differential mode). If COM is clear then differential mode is set, and each conversion will be the measurement between the IN+ and IN- pins.

Gain2:0: If BASIC or non-sequenced mode is configured via the SEQ1:0 bits then Gain2:0 selects the gain to be used for the conversion(s) commanded. If advanced sequence mode is configured then these bits are ignored (bits 2:0 at +18 take precedence in advanced sequencer mode)

/MUX: All users should set this bit to "1" unless otherwise instructed by the factory. If MUX is clear (0) then the conversion will be from the auxiliary mux inputs (in non-sequencer mode) or the sequence will include the aux input (sequencer modes). Not recommended.

SEQ1:0: Use "00" for non-sequenced mode and "10" for advanced sequencer mode. "11" sets basic sequencer mode, and "01" updates the basic sequence-in-progress. Not recommended.

/TEMP: If TEMP is clear (0) then the conversion will be from the onboard temperature reference (in non-sequencer mode) or the sequence will include the temperature input (sequencer modes). Not recommended. Most users should set this bit to 1.

CMS: Must be set if conversion will occur slower than 1kHz. Must be clear if conversions will occur faster than 900kHz.

IRQ Enable/Clear and Status, Offset +40 of 64-bit Memory BAR[2+3] Read/Write 32-bits only																				
bit	D31	D30 … D24	D23	D22	D21	D20	D19	D18	D17	D16	D15 … D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	WDG	UNUSED	EXT	LDAC	FOF	FAF	DTO	DDONE	ADCSTART	ADCTRIG	UNUSED	enEXT	enLDAC	enFOF	enFAF	enDTO	enDDONE	enADCSTART	enADCTRIG

Read IRQ Status to determine which/if any IRQs have fired (D23…D16), if the Watchdog has Barked (D31), and which IRQs are enabled (D7…D0):

WDG: If WDG is SET then the Watchdog Timer has Barked (timed out). Refer to Watchdog Control (+4C) for details on using the Watchdog Timer feature.

EXT: If EXT is SET then an IRQ has been fired from the DIO13 Secondary Function "External IRQ". Refer to DIO Control (+48) for details on DIO Secondary Functions.

LDAC: If LDAC is SET then an IRQ has been fired from the DIO12 Secondary Function "LDAC". Refer to DIO Control (+48) for details on DIO Secondary Functions.

FOF: If FOF is SET then an IRQ has been fired because the ADC FIFO has Overrun: More data was acquired than fit in the ADC FIFO.

FAF: If FAF is SET then an IRQ has been fired because the ADC FIFO Count (+28) has reached the configured FIFO Almost Full IRQ Threshold (+20).

DTO: If DTO is SET then a DMA Timeout IRQ has been fired.

DDONE: If DDONE is SET then a DMA Done IRQ has been fired.

ADCSTART: If ADCSTART is SET then an IRQ has been fired from the DIO14 Secondary Function "ADCSTART". Refer to DIO Control (+48) for details on DIO Secondary Functions.

ADCTRIG: If ADCTRIG is SET then an IRQ has been fired from the DIO15 Secondary Function "ADCTRIG". Refer to DIO Control (+48) for details on DIO Secondary Functions.

Bits D7 through D0 indicate if the corresponding IRQ has been enabled.

Write IRQ Status bits SET to clear the latched IRQ Status bit(s). Typically, code will read +40 and write the value to +40 to clear all detected IRQs and leave the IRQ enables unchanged.

Write IRQ Enable bits SET to enable corresponding IRQ sources.

DIO Data, Offset +44 of 64-bit Memory BAR[2+3] Read/Write 32-bits only																	
bit	D31 through D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	UNUSED	DIO15	DIO14	DIO13	DIO12	DIO11	DIO10	DIO9	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
I/O GROUP		8	7	6	5	4	3	2	1	I/O Group 0							

Read DIO Data to read the digital input pins or to readback the last commanded digital output state.

Write to DIO Data to configure the digital pin(s)' high/low state for those bits in I/O Groups configured as Outputs. SET bits will output high voltage, CLEAR bits will output GND.

Refer to DIO Control (+48) for how to configure the input vs output direction of each I/O Group.

DIO Control, Offset +48 of 64-bit Memory BAR[2+3] Read/Write 32-bits only																				
bit	D31…D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7 through D1	D0
Name	UNUSED	enWDT	edgeEXT	enEXT	edgeLDAC	enLDAC	edgeSTART	enSTART	edgeTRIG	enTRIG	IOG8	IOG7	IOG6	IOG5	IOG4	IOG3	IOG2	IOG1	UNUSED	IOG0

Write DIO Control to enable Digital Secondary Functions, and to control the input vs output direction of each Digital I/O Group.

enWDG: SET enWDT to enable the "WDT Output Status" Digital Output Secondary Function on DIO 11. DIO 11 (I/O Group 4) becomes an output and indicates the state of the Watchdog Feature.

enEXT: SET enEXT to enable the "External IRQ" Digital Input Secondary Function on DIO 13 so the selected edge on the input will (optionally) generate IRQs.

enLDAC: SET enLDAC to enable the "External LDAC" Digital Input Secondary Function on DIO12 so the selected edge will cause the DACs to update and optionally generate an IRQ.

enSTART: SET enSTART to enable the "ADC Start Conversion" Digital Input Secondary Function on DIO 14 so the selected edge will cause an ADC Start Event and optionally generate an IRQ.

enTRIG: SET enTRIG to enable the "ADC Trigger" Digital Input Secondary Function on DIO15 so the selected edge will trigger timed ADC conversions and optionally generate an IRQ. Consult the "Software Tips" section for details on using ADC Trigger.

Each Digital Input Secondary function has a configurable active edge, rising or falling. SET the corresponding edge*XXX* bit to select rising edge, CLEAR the bit for falling edge.

IOG*x*: SET each IOGx bit to configure the digital I/O bits in the associated I/O Group for use as digital outputs. CLEAR an IOG*x* bit to configure the I/O Group for use as inputs.

DAC Waveform FIFO, Offset +50 of 64-bit Memory BAR[2+3] Read/Write 32-bits only	
DAC Waveform FIFO:	Write DAC commands to load the DAC Waveform FIFO. Generally 0x000nCCCC where n is the DAC# and CCCC is the counts. Read returns the number of control values currently in the FIFO.

DAC Waveform DACs/Point, Offset +54 of 64-bit Memory BAR[2+3] Read/Write 32-bits only	
DAC Waveform DACs/Point:	Write 1, 2, 3 or 4 to specify how many DACs are being used for Waveform Playback.

DAC Waveform FIFO Size, Offset +58 of 64-bit Memory BAR[2+3] Read 32-bits only	
DAC Waveform FIFO Size:	Read to determine the DAC Waveform FIFO size in 32-bit DAC command values. Typically 0x2000, or 8192 values.

In Windows[1], please consult the various samples (C#, Delphi, and more) to explore how to program the device. The AIOAIO Software Reference Manual.pdf provides reference material covering all AIOAIO Library APIs.

Under certain circumstances the following information might prove useful:

PCI Express Mini Card Plug-and-Play Data	
BAR[n]	Description
1:0	DMA Registers
3:2	I/O Registers

A NOTE ABOUT PERFORMANCE

The PCI Express bus and the PCI Express Mini Card standard are capable of very high bandwidth, but the latency per-transaction is roughly the same as all the other busses – it hasn't improved in decades. This means you can expect to usually see a not-less-than 1MHz transaction rate. Typical rates exceed 3MHz [0.3µs].

Unfortunately, modern Operating Systems have introduced a new source of latency, the kernel / userland division. Application code runs in userland, which must transition to the kernel in order to perform any hardware operation. This transition adds quite a lot of latency, which varies between different OSes, motherboards and revisions thereof, etcetera. A Windows XP system can see an additional 7µs per transaction; a modern computer might see 3µs or less. Any transaction from the kernel itself, however, avoids this additional overhead.

Real-time operating systems will enable the highest transaction rates possible, all the way up to the hardware limits.

PCI Express Mini Card Plug-and-Play Data	
Vendor / Device ID	**Card Type**
0x494F / 0x0100	mPCIe DIO Base

Available Downloads

The latest information can always be found on the product page on the website. Here are some useful links:

Links and useful downloads	
Main site	http://accesio.com
Product's page	accesio.com/mPCIe-DAAI16-8F
This manual	accesio.com/MANUALS/mPCIe-DAAI16-8F.pdf
Windows Software Install Package	accesio.com/files/packages/mPCIe-DAAI16-8F Install.exe

[1] *In Linux or OSX please refer to the documentation at* github.com/accesio/apci.

Chapter 8: Specifications

PC Interface

PCI Express Mini Card	Type F1 "Full Length", double-stack

Analog Outputs

Number	8
Type:	Single-ended Voltage, Current
Resolution:	16-bit
Voltage Ranges:	0-5V, 0-10V, ±5V, ±10V (with software enabled 20% overrange)
Current Ranges:	4-20mA, 0-20mA, 0-24ma
Settling Time	20us typical, +/-10V (+/-1LSB at 16 bits)
Output Current	max ±10mA per channel

Analog Inputs

ADC Type	Successive approximation
Resolution	16-bit differential bipolar ADC
Sampling rate	1 MSPS aggregate
Number of channels	8 SINGLE-ENDED or 4 DIFFERENTIAL (software selectable)
Differential Bipolar Ranges (V)	±12, ±10, ±5, ±2.5, ±1.25, ±0.625, ±0.3125V with 0, 0, ±5.12, ±7.68, ±8.96, ±9.60, ±9.92V common mode rejection, respectively
4-20mA or 10-50mA	Factory options
Int Nonlinearity Error	±0.6 LSB to ±1.5 LSB depending on gain
No Missing Codes	16 bits
Input Impedance	>500MΩ
A/D Start Sources	Software Start, Timer Start, External Start, Externally Triggered Timer Start
A/D Start Types	Single Channel or Scan
Overvoltage Protection	Current limiting through 2 KΩ
Crosstalk	-120dB @ 10kHz

Environmental

Temperature	Operating	0°C to +70°C -40°C to +85°C (-T option)
	Storage	-40°C to +105°C
Humidity		5% to 95% RH, non-condensing
Dimensions	Length	50.95mm (2.006")
	Width	30.00mm (1.181")
	Height	0.5 " (2 card stack plus connector)
Weight	12g	

Digital Input / Output Interface

Digital Bits		4 inputs and 4 outputs
Performance		1 µs per transaction max (~3.5µs in non-kernel Windows, typ.)
Digital Inputs	Logic High Logic Low	2.0V to 3.3VDC (5VDC tolerant) 0V to 0.8V
Digital Outputs	Logic High Logic Low	2.0V (min) 24mA source 0.55V (max) 24mA sink

Power

Power required (from mPCIe Bus)	+3.3VDC @ 150mA (idle) +1.5VDC @ 200mA (idle)

I/O Interface Connectors

DAC	On card	Molex 5011902017 20-pin latching
	Mating	Molex 5011892010 20-pin latching
ADC + DIO	On card	Molex 5011903017 30-pin latching
	Mating	Molex 5011893010 30-pin latching

Model Options

-T	Extended Temperature Operation (-40° to +85°C)
-I or -ID	4-20mA inputs (single-ended or differential)
-Sxx	Special configurations (10-50mA inputs, input voltage dividers, conformal coating, etc.)

Chapter 9: Certifications

CE & FCC

These devices are designed to meet all applicable EM interference and emission standards. However, as they are intended for use installed on motherboards, and inside the chassis of industrial PCs, important care in the selection of PC and chassis is important to achieve compliance for the computer as a whole.

UL & TUV

No AC or DC voltages above 31V are consumed or produced during normal operation of this device. This product is therefore exempt from any related safety standards. Use it with confidence!

ROHS / LEAD-FREE STATEMENT

All models are produced in compliance with RoHS and various other lead-free initiatives.

WARNING

A SINGLE STATIC DISCHARGE CAN DAMAGE YOUR CARD AND CAUSE PREMATURE FAILURE! PLEASE FOLLOW ALL REASONABLE PRECAUTIONS TO PREVENT A STATIC DISCHARGE SUCH AS GROUNDING YOURSELF BY TOUCHING ANY GROUNDED SURFACE PRIOR TO TOUCHING THE CARD.

ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A CARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING CARDS, INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O CARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

WARRANTY

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations:

GENERAL

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arriving from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to

ACCES equipment not approved in writing by ACCES or, if in ACCES opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.

TERMS AND CONDITIONS

If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

COVERAGE

FIRST THREE YEARS: Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment.

FOLLOWING YEARS: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

EQUIPMENT NOT MANUFACTURED BY ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

DISCLAIMER

The information in this document is provided for reference only. ACCES does not assume any liability arising out of the application or use of the information or products described herein. This document may contain or reference information and products protected by copyrights or patents and does not convey any license under the patent rights of ACCES, nor the rights of others