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MODEL 104-QUAD-8
MODEL 104-QUAD-6
MODEL 104-QUAD-4

EIGHT, SIX AND FOUR CHANNEL QUADRATURE INPUT PC/104 BOARDS

USER MANUAL

File: M104-QUAD-8.D1d

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TABLE OF CONTENTS

Chapter 1: Introduction

Features

- Up to eight quadrature encoders may be connected
- Input conditioning per channel allows a variety of encoder types to be used
- Interrupt for an encoder index is program enabled per channel
- Outputs to computer can include count, direction of movement
- 24 bit counters for each input channel
- +5V supply available to the user

Applications

- Automatic Test Systems
- Laboratory Automation
- Robotics
- Machine Control
- Security Systems
- Energy Management

Functional Description

The card is a general purpose Quadrature Encoder Counter/Interface board. It is provided in the popular PC/104 format and conditions and monitors the outputs of 8 encoders.

Available functions include anything that can be programmed into the versatile LSI/CSI LS7267 integrated circuit. Core functions handled by the LS7267 includes direction and total count. By performing these functions on-board, it frees the computer for higher level applications.

The ability to provide an interrupt for the index frees the computer from the necessity of constantly reading the position of an encoder.

Interrupts are directed to levels #2 through #7, #10 through #12, and #15 by jumper installation.

The card is designed for industrial applications. Each input line is buffered and capable of accepting inputs up to 6 volts. A +5 Volt source is available to provide power for many encoder types.

The conditioned inputs are connected to associated LSI/CSI LS7267 integrated circuits. These circuits are the heart of the card's operation. We strongly recommend reviewing the manufacturer's data sheet for detailed information.

The card occupies 32 bytes of I/O address space. The base address is selectable via jumpers anywhere within the range of 100-3E0 hex. An illustrated setup program is provided with the card. Interactive displays show locations and proper settings of jumpers to set up board address and interrupt levels.

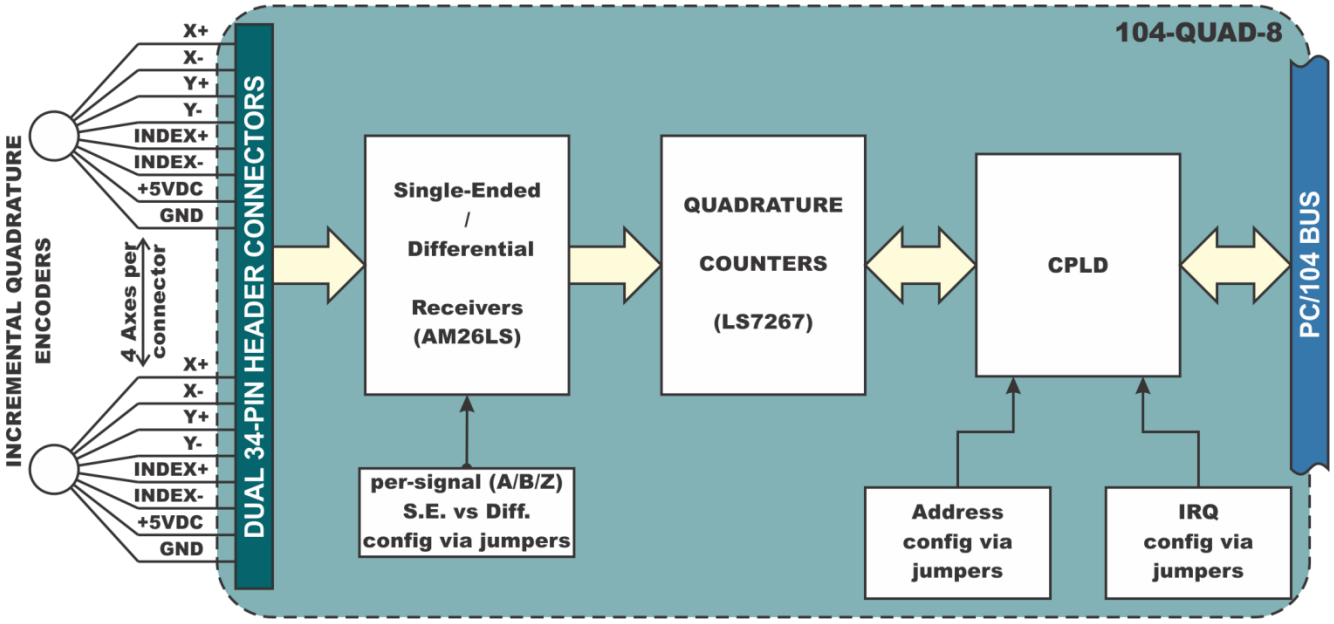


Figure 1-1: Block Diagram

Ordering Guide

104-QUAD-8	Eight-channel quadrature decoder PC/104 board
104-QUAD-6	Six-channel quadrature decoder PC/104 board
104-QUAD-4	Four-channel quadrature decoder PC/104 board

Model Options

- -T Extended operating temperature of -40° to +85°C
- -RoHS This product is available in a RoHS compliant version. Please call for specific pricing then be sure to add this suffix to the model number on any hard-copy or verbal purchase orders.

Included with your board

The following components are included with your shipment, depending on options ordered. Please take the time now to ensure that no items are damaged or missing.

- PC/104 quadrature board

Optional Accessories

- C104-34F-12 Ribbon cable assembly, 12” with 34 pin female headers on each end
- STB-34 Screw terminal board, 34 pin male header
- DIN-SNAP6 DIN-rail mounting for one STB-34
- 104-HDW-KIT(x) PC/104 mounting hardware kit includes standard 4/40 (x=S for standard), (x=M for metric) standoffs and pan-head Phillip screws for securing into PC/104 stack

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the board for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this PC/104 Board is available for download from the product page on our website at http://ACCES.IO/Downloads. It is also optionally available for a nominal cost on CD (must specify when ordering product) and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your CD-ROM where you see d: in the examples below.

CD Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

Windows

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D:\INSTALL, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

Linux

1. Please visit https://github.com/accesio/Linux_PC104_legacy for Linux support for this board family. Also, you may refer to linux.htm on the optional CD-ROM for information on installing under linux.

Installing the Hardware

Before installing the board, carefully read Chapter 3 and Chapter 4 of this manual and configure the board according to your requirements. The SETUP Program can be used to assist in configuring jumpers on the board. Be especially careful with Address Selection. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. To help avoid this problem, refer to the FINDBASE.EXE program installed from the CD. The setup program does not set the options on the board, these must be set by jumpers.

To Install the Board

1. Install jumpers for selected options and base address according to your application requirements, as mentioned above.
2. Remove power from the PC/104 stack.
3. Assemble standoff hardware for stacking and securing the boards.
4. Carefully plug the board onto the PC/104 connector on the CPU or onto the stack, ensuring proper alignment of the pins before completely seating the connectors together.
5. Install I/O cables onto the board's I/O connectors and proceed to secure the stack together or repeat steps 3-5 until all boards are installed using the selected mounting hardware.
6. Check that all connections in your PC/104 stack are correct and secure then power up the system.
7. Run one of the provided sample programs appropriate for your operating system that was installed from the CD to test and validate your installation.

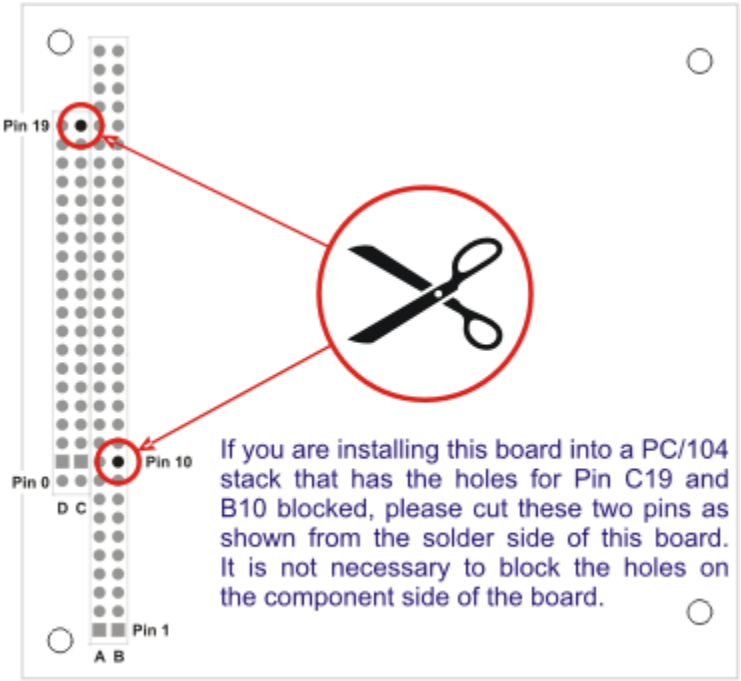


Figure 2-1: PC/104 Key Information

Chapter 3: Option Selection

The only selections necessary to setup on the card are the card's base address and the differential (DIFF) / single-ended (SE) jumpers. All other features are setup via software, except IRQ's.

Interrupts are optional, and directed to levels #2 through #7, #10 through #12, and #15 by a jumper at locations labeled IRQ2 through IRQ7, IRQ10 through IRQ12, and IRQ15.

For PCB Revision C1 and newer, the "Input Mode Select" for encoder output type has 3 jumpers per channel, 1 each for A, B & Z (Index).

From the center jumper post to the "SE" position applies 1.4V to receiver low inputs.
From the center jumper post to the "DIFF" position applies 1KΩ Termination between high and low inputs and completes open wire detection circuitry.

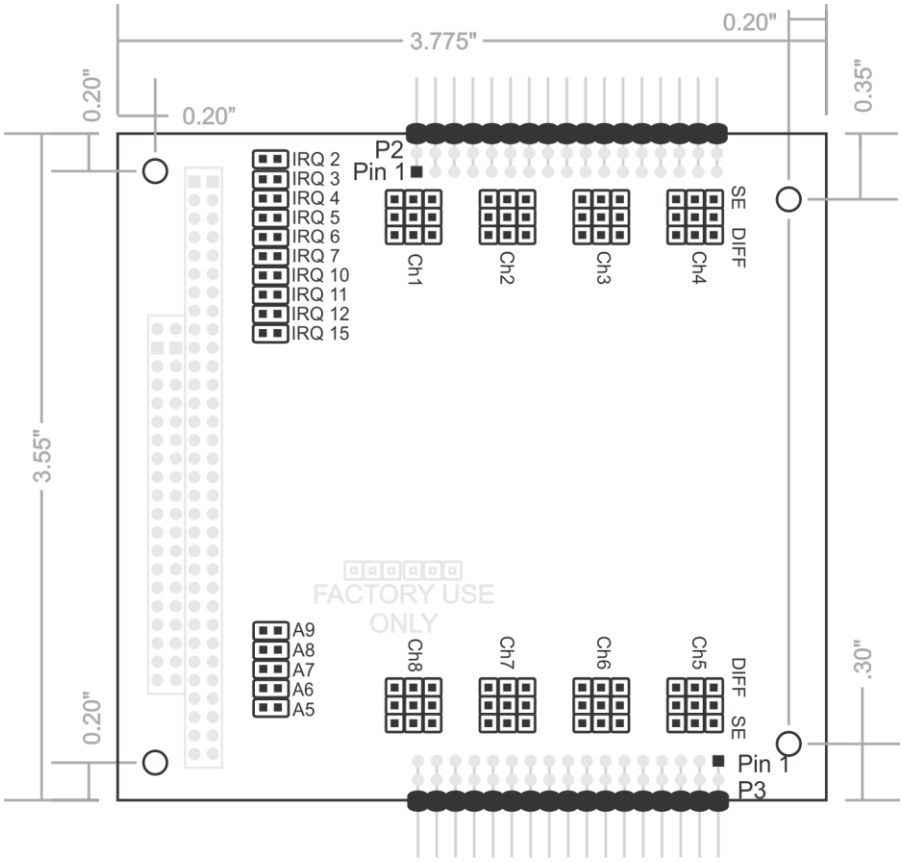


Figure 3-1: Setup Configuration Map

Chapter 4: Address Selection

The card occupies 32 bytes of I/O space. The card base address can be selected anywhere within the I/O address range 100-3E0 hex. If in doubt of where to assign the base address, refer to the table below and the FINDBASE program.

HEX RANGE	USAGE
000-00F	8237 DMA Controller 1
020-021	8259 Interrupt
040-043	8253 Timer
060-06F	8042 Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Register
0A0-0BF	8259 Slave Interrupt Controller
0C0-0DF	8237 DMA Controller 2
0F0-0F1	Math Coprocessor
0F8-0FF	Math Coprocessor
170-177	Fixed Disk Controller 2
1F0-1F8	Fixed Disk Controller 1
200-207	Game Port
238-23B	Bus Mouse
23C-23F	Alt. Bus Mouse
278-27F	Parallel Printer
2B0-2BF	EGA
2C0-2CF	EGA
2D0-2DF	EGA
2E0-2E7	GPIB (AT)
2E8-2EF	Serial Port
2F8-2FF	Serial Port
300-30F	
310-31F	
320-32F	Hard Disk (XT)
370-377	Floppy Controller 2
378-37F	Parallel Printer
380-38F	SDLC
3A0-3AF	SDLC
3B0-3BB	MDA
3BC-3BF	Parallel Printer
3C0-3CF	VGA EGA
3D0-3DF	CGA
3E8-3EF	Serial Port
3F0-3F7	Floppy Controller 1
3F8-3FF	Serial Port

Table 4-1: Hex Ranges

The board's base address is set up by JUMPERS. Those jumpers control address bits A5 through A9. (Lines A4, A3, A2, A1 and A0 are used on the board to control individual registers. How these four lines are used is described in the Programming section of this manual.)

To determine how to set these JUMPERS for a desired hex-code address, refer to the SETUP program provided with the board. If you prefer to determine proper jumper settings yourself, first convert the hex-code address to binary form. Then, for each "0", install corresponding jumpers and for each "1", remove the corresponding jumper.

The following example illustrates jumper selection corresponding to hex 300 (or binary 11 000x xxxx). The "x xxxx" represents address lines A4, A3, A2, A1, and A0 used on the board to select individual registers as described in the Programming section of this manual.

Base Address in Hex Code	3		0		
Conversion Factors	2	1	8	4	2
Binary Representation	1	1	0	0	0
Jumper Legend	A9	A8	A7	A6	A5
Addr. Line Controlled	A9	A8	A7	A6	A5
Jumper Selection	OFF	OFF	ON	ON	ON

Table 4-2: Hex Conversion Table

Carefully review the address selection reference table on the preceding page before selecting the board address. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior.

Chapter 5: Programming

The card is an I/O-mapped device that is easily configured from any language and any language can easily perform quadrature reads. This is especially true if the form of the data is byte or word wide. All references to the I/O ports would be in absolute port addressing. However, a table could be used to convert the byte or word data ports to a logical reference.

Please refer to the chip-specification for the LS7267 in addition to this user manual for guidance and information helpful to write device drivers for it (this spec sheet is on the software CD located in "ChipDocs"), Also, the source code for Windows shows how to write device drivers for this product.

Address	Port Assignment	Operation	Device
Base Address	Channel 1 Data	Read/Write	First LS7267
Base Address +1	Channel 1 Flag / Command	Read/Write	
Base Address +2	Channel 2 Data	Read/Write	
Base Address +3	Channel 2 Flag / Command	Read/Write	
Base Address +4	Channel 3 Data	Read/Write	Second LS7267
Base Address +5	Channel 3 Flag / Command	Read/Write	
Base Address +6	Channel 4 Data	Read/Write	
Base Address +7	Channel 4 Flag / Command	Read/Write	
Base Address +8	Channel 5 Data	Read/Write	Third LS7267
Base Address +9	Channel 5 Flag / Command	Read/Write	
Base Address +A	Channel 6 Data	Read/Write	
Base Address +B	Channel 6 Flag / Command	Read/Write	
Base Address +C	Channel 7 Data	Read/Write	Fourth LS7267
Base Address +D	Channel 7 Flag / Command	Read/Write	
Base Address +E	Channel 8 Data	Read/Write	
Base Address +F	Channel 8 Flag / Command	Read/Write	
Base Address +10	Interrupt Status Register	Read Only	CPLD
Base Address +11	Channel Operation Register	Read/Write	
Base Address +12	Index/Interrupt Register	Read/Write	
Base Address +13	Reserved for Factory Use	N/A	
Base Address +14	Reserved for Factory Use	N/A	
Base Address +15	Reserved for Factory Use	N/A	
Base Address +16	Index Input Levels	Read Only	
Base Address +17	Differential Encoder Cable Status	Read/Write	
Base Address +18	CPLD Revision	Read Only	
Base Address +19 through +1F	Reserved for Factory Use	N/A	

Table 5-1: Base Address Map

Data Registers (0, 2, 4, 8, A, C, E)h:

These registers are read to retrieve the current count from the channel, and written to set the Preset Register and the Filter Clock Prescalers.

To get the count from Channel 1 (Data register 0) you would first write 11h to the control register at address 1. Three reads are then required to get the current count from data register 0. The first read returns the Least Significant Byte and the last read returns the Most Significant Byte.

In order to write to the Preset Register first write 11h to the control register. Then perform three writes to the data register. The first write is the Least Significant Byte, and the last write is the Most Significant Byte.

In order to write to the Filter Clock Prescaler first write 11h to the control register. Then write one byte to the data register with the desired PSC value. Then write 19h to the control register.

Control Registers (1, 3, 5, 7, 9, B, D, F)h:

The control registers all correspond to the data register that is one address below it.
The control register is used for the following operations:

- Reading the Flag Register;
- Resetting the BP (three byte data pointer) and flags;
- Setting the PSC (filter clock factor n) and PR (preset count);
- Initial setup of the Counter Mode Register, Input/Output Control Register and Index Control Register.

Reading the FLAG Register:

Bit 0 BT: Borrow Toggle flip-flop. Toggles every time the counter underflows.

Bit 1 CT: Carry Toggle flip-flop. Toggles every time the counter overflows.

Bit 2 CPT : Compare Toggle flip-flop. Toggles every time the counter is equal to the Preset Register.

Bit 3 S: Sign flag. Set to 1 when counter underflows and reset to 0 when it overflows.

Bit 4 E: Error flag. Set to 1 when excessive noise is present at the count inputs in quadrature mode. Ignore in other modes.

Bit 5 U/D: Up/Down flag. Set to 1 when counting up and reset to 0 when counting down.

Bit 6 IDX: Index. Set to 1 when selected index input is at active level.

Bit 7: Not used is always 0.

Writing to the RLD (Reset and Load Signal Decoders):

Bit 0: 1 to reset BP.

Bits 1 & 2: Set bit 1 high to reset CNTR, set bit 2 high to reset BT, CT, CPT, S flags.
Set both bits high to reset E flag.

Bits 3 & 4: Set bit 3 high to transfer Preset Register to Counter.
Set bit 4 high to transfer CNTR to Output Latch.
Set both high to transfer Preset Register LSB to the PSC (FCK Prescaler).

Bits 5 & 6: Set both bits to 0.

Bit 7: Set high to program both counters simultaneously.

Writing to the CMR (Counter Mode Register):

Bit 0: Set low to use Binary count, and set high to use BCD count.

Bits 1 & 2: Set both low to use Normal count.
Set bit 1 high to use Range Limit.
Set bit 2 high to use Non-Recycle count.
Set both bits high to use Modulo-N count.

Bits 3 & 4: Set both bits low to use non-quadrature mode.
Set bit 3 high to use Quadrature times 1.
Set bit 4 high to use Quadrature times 2.
Set both bits high to use Quadrature times 4.

Bits 5 & 6: Set bit 5 high and bit 6 low.

Bit 7: Set high to program both counters simultaneously.

Writing to the IOR (Input / Output Control Register):

Bit 0: Set high to enable A and B inputs.

Bit 1: Set low to preset count when Index occurs.
Set high to continuously count.

Bit 2: Set low.

Bits 3 & 4: Set both bits low to use FLG1 as /Carry (active low).
Set bit 3 high to use FLG1 as /Compare (active low).
Set bit 4 high to use FLG1 as /Carry/Borrow (active low).
Set both bits high to use FLG1 as Index (active high).

Bits 5 & 6: Set bit 5 low and bit 6 high.

Bit 7: Set high to program both counters simultaneously.
Note that when Interrupts are enabled on the card they occur whenever FLG1 is active.

Writing to the IDR (Index Control Register):

Bit 0: Set high to enable index.

Bit 1: Set high for a positive index polarity.
Set low for a negative index polarity.

Bit 2: Set low.

Bits 3 & 4: Not used.

Bits 5 & 6: Set high.

Bit 7: Set high to program both counters simultaneously.

Working with Interrupts:

Reading the Interrupt Status Register (10h)

When an interrupt occurs read from address 10h to determine which channel was the source.

Bit 0-7: The Least Significant Bit will correspond to the first channel.
High = true

Writing to the Channel Operation Register (11h)

Any write to this address will clear any pending interrupts.
A read from this address will return it's contents.

Bit 0: Set high to reset all Counters.
Set low to enable all Counters.

Bit 1: Reserved.

Bit 2: Set low to disable the interrupt function.
Set high to enable the interrupt function.

Bits 3-7: Reserved.

Writing to the Index / Interrupt Register (12h)

This register is used to Preset Counter via the LCNTR input pin when a channel index occurs as described in **Writing to the IOR** and **Writing to the IDR**.

Additionally it is used to generate interrupts whenever FLG1 on a channel is active as described in **Writing to the IOR** and **Writing to the Channel Operation Register.**

Each bit of this register enables / disables a corresponding channel.
A read from this address will return it's contents.

Bit 0: Set high to enable Channel 1
Bit 1: Set high to enable Channel 2
Bit 2: Set high to enable Channel 3
Bit 3: Set high to enable Channel 4
Bit 4: Set high to enable Channel 5
Bit 5: Set high to enable Channel 6
Bit 6: Set high to enable Channel 7
Bit 7: Set high to enable Channel 8

Reading Index Input Levels (16h)

Bit 0 through 7 correspond to channels 1 through 8.
Logic 0 = Index Input low (false).
Logic 1 = Index Input high (true).
*If your encoder does not have an Index signal, the Index Positive Input pin needs to be grounded or the corresponding channel bit will return a logic 1 level.

Reading Differential Encoder Cable Status (17h)

Bit 0 through 7 correspond to channels 1 through 8.
To enable any channel write a 0 to the corresponding bit.
When enabled, Logic 0 = cable fault (not connected or loose wires).
Logic 1 = cable connection good or cable fault disabled (default).
Bits 0 through 7 will always read a high when disabled.

Reading the CPLD Revision Register (18h)

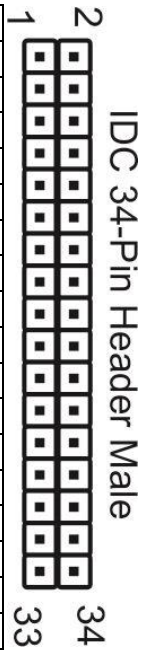
To determine the CPLD Revision read from address 18h
Old card revisions B10 and earlier will read FF
Revision C1 cards will read 00
Revision C2 cards will read 01

Sample Code (C:DOS / debug.exe)

Channel 1 setup
o 301 15
o 300 00
o 300 00
o 300 00
o 301 28
o 301 59
o 301 63
o 311 05
o 311 04
o 312 01
Channel 1 data (24-bit) and flags (8-bit), card interrupt status (8-bit)
o 301 11
i 300
i 300
i 300
i 301
i 310
o 311 04
repeat above 7 commands while turning encoder

Chapter 6: Connector Pin Assignments

Function	CH#	Pin
Ground	1	1
Index Negative Input	1	3
Quadrature A Negative Input	1	5
Quadrature B Negative Input	1	7
Ground	2	9
Index Negative Input	2	11
Quadrature A Negative Input	2	13
Quadrature B Negative Input	2	15
Ground	3	17
Index Negative Input	3	19
Quadrature A Negative Input	3	21
Quadrature B Negative Input	3	23
Ground	4	25
Index Negative Input	4	27
Quadrature A Negative Input	4	29
Quadrature B Negative Input	4	31
No connection		33



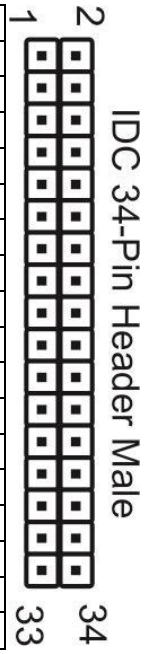
Pin	CH#	Function
2	1	Fused +5V
4	1	Index Positive Input
6	1	Quadrature A Positive Input
8	1	Quadrature B Positive Input
10	2	Fused +5V
12	2	Index Positive Input
14	2	Quadrature A Positive Input
16	2	Quadrature B Positive Input
18	3	Fused +5V
20	3	Index Positive Input
22	3	Quadrature A Positive Input
24	3	Quadrature B Positive Input
26	4	Fused +5V
28	4	Index Positive Input
30	4	Quadrature A Positive Input
32	4	Quadrature B Positive Input
34		No connection

Table 6-1: Connector Pin Assignments - P2

Notes:

1. When using single-ended Encoders leave the Negative Input open (internal 1.4V threshold level) and connect the Encoder (A, B, Index) output lead to the corresponding Positive Input pin.
2. Both single-ended and differential Encoders require a ground connection between the Encoder and the PC/104 board to eliminate the adverse effects of exceeding the common mode range when an external power supply is used.
3. When the Fused +5V source is used to power your encoders, (i.e. on pins 2, 10, 18, & 26) Ground (i.e. on pins 1, 9, 17, & 25) is a required return path.

Function	CH#	Pin
Ground	5	1
Index Negative Input	5	3
Quadrature A Negative Input	5	5
Quadrature B Negative Input	5	7
Ground	6	9
Index Negative Input	6	11
Quadrature A Negative Input	6	13
Quadrature B Negative Input	6	15
Ground	7	17
Index Negative Input	7	19
Quadrature A Negative Input	7	21
Quadrature B Negative Input	7	23
Ground	8	25
Index Negative Input	8	27
Quadrature A Negative Input	8	29
Quadrature B Negative Input	8	31
No connection		33



Pin	CH#	Function
2	5	Fused +5V
4	5	Index Positive Input
6	5	Quadrature A Positive Input
8	5	Quadrature B Positive Input
10	6	Fused +5V
12	6	Index Positive Input
14	6	Quadrature A Positive Input
16	6	Quadrature B Positive Input
18	7	Fused +5V
20	7	Index Positive Input
22	7	Quadrature A Positive Input
24	7	Quadrature B Positive Input
26	8	Fused +5V
28	8	Index Positive Input
30	8	Quadrature A Positive Input
32	8	Quadrature B Positive Input
34		No connection

Table 6-2: Connector Pin Assignments - P3

Notes:

1. When using single-ended Encoders leave the Negative Input open (internal 1.4V threshold level) and connect the Encoder (A, B, Index) output lead to the corresponding Positive Input pin.
2. Both single-ended and differential Encoders require a ground connection between the Encoder and the PC/104 board to eliminate the adverse effects of exceeding the common mode range when an external power supply is used.
3. When the Fused +5V source is used to power your encoders, (i.e. on pins 2, 10, 18, & 26) Ground (i.e. on pins 1, 9, 17, & 25) is a required return path.

Chapter 7: Specification

Power Consumption

▪ + 5 Volts	260mA (typical, no load on +5V fused output pins)
+ 5 V Fused Outputs	Two 0.5A Resettable fuses

Input Section

▪ Receiver Type	AM26LS32
▪ Configuration per Encoder	Phase A, Phase B and Index
▪ Number of Channels	4 or 8
▪ Common mode input range	+/- 7 V maximum
▪ Differential Input Range	+/- 25 V maximum Differential voltage values are at the noninverting (+) input terminals with respect to the inverting (-) input terminals
▪ Sensitivity	+/- 200 mV
▪ Hysteresis	50 mV typical
▪ Termination	1k Ω when differential jumper is installed
▪ Input bias	(Positive pins) 100kΩ to +5V (Negative pins) 100kΩ to ground
▪ Single-ended threshold	(Negative pins) +1.4V via pull up/down combo Only when single-ended jumper is installed (Rev C PCBs and newer)

Counter Section

▪ Counter Type:	LS7267 24 bit Dual Axis Quadrature Counter
▪ Quadrature Clock Frequency	4.3 MHz maximum
▪ Quadrature Separation	57 ns min
▪ Quadrature Clock Pulse Width	115 ns min
▪ Index Pulse width	85 ns min
▪ Filter Clock (FCK)	PC/104 Bus OSC 14.318 MHz

Interrupt Controller Section

▪ Controller Type	CPLD
▪ Interrupts	Jumper selectable (2-7,10-12,15)
▪ Interrupt Sources	FLG1 outputs from LS7267
▪ Addressing	ISA bus address is set by jumpers (100-3E0h)

Environmental

▪ Operating Temperature:	0˚C to +70˚C (optional -40˚C to +85˚C)
▪ Storage Temperature:	-50˚C to +120˚C
▪ Humidity:	up to 95% RH, non-condensing

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com***. Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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