16 Analog input, 4 Analog Output for Mini PCI Express Hardware Manual

Models **mPCIe-AIO16-16F Family**

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Chapter 1: Quick Start

It is recommended that you install the software package before installing the PCI Express Mini Card (mPCIe) in your computer. You can install the software[1] using either a stand-alone installer downloaded from the website or an optional Software Master CD.

Run the installer you downloaded (or autorun.exe on the Software Master CD) and follow the prompts to install the software for your device.

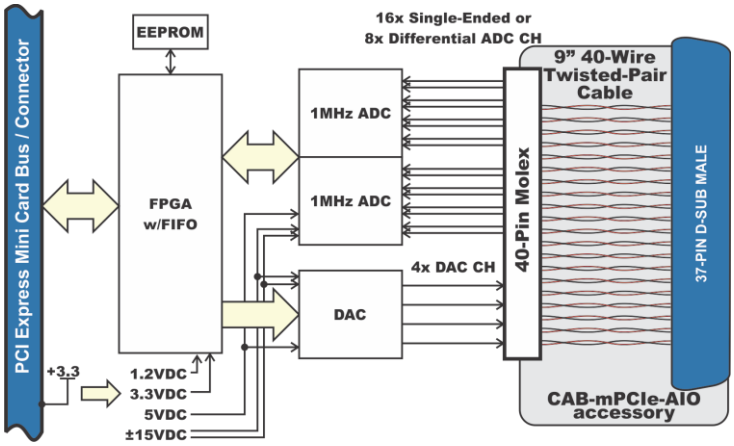
Please note: during the installation you may be prompted regarding the installation of non-WHQL-certified drivers; please carefully confirm the digitally signed source of the drivers and accept the installation.

Once the software has been installed, shut down your system and carefully install the mPCIe card.

Re-start your system. Once the computer finishes booting, your new digital I/O should already be installed and ready for use; you can confirm this by launching Device Manager and looking under the "Data Acquisition" section. If, for any reason, the device displays a warning triangle, right-click and select "Update Driver".

[1] In Linux or OSX please refer to the instructions in those directories.

Chapter 2: Introduction



PCI Express Mini Card (mPCIe), a low-profile small-footprint bus standard originally intended for adding peripherals to notebook computers, has become the de-facto standard for high-performance, small form-factor devices in many applications.

- PCI Express Mini Card (mPCIe) type F1, with latching I/O connector
- 16-bit, Bipolar, Differential, A/D converters
  - Software selectable as 16+0, 8+4, or 0+8 (Single-Ended + Differential Inputs)
  - 7 channel-by-channel programmable differential input ranges from ±0.64V up to ±24.576V
  - Sustained sampling rates up to 1MHz (2Msps)
  - A/D starts via software or periodic hardware timer
  - Ease of use—16-bit, 2MSPS complete data acquisition system
  - High impedance, 8-channel input: 1 MΩ
- Four 16-bit analog outputs
  - 5 per-channel programmable ranges: 0V to 5V, 0V to 10V, ±2.5V, ±5V, ±10V
  - Outputs Drive ±10mA Guaranteed
- RoHS compliant standard

Chapter 3: Hardware

This manual applies to the following models:		VENDEV
mPCIe-AIO16-16F	mPCIe, A/D 16-bit, 2MHZ, 4 D/A	494F:C0E8
mPCIe-AIO16-16A	mPCIe, A/D 16-bit, 500KHZ, 4 D/A	494F:C0E9
mPCIe-AIO16-16E	mPCIe, A/D 16-bit, 250KHz, 4 D/A	494F:C0EA
mPCIe-AI16-16F	mPCIe, A/D 16-bit, 2MHZ	494F:80E8
mPCIe-AI16-16A	mPCIe, A/D 16-bit, 500KHZ	494F:80E9
mPCIe-AI16-16E	mPCIe, A/D 16-bit, 250KHz	494F:80EA
mPCIe-AIO12-16A	mPCIe, A/D 12-bit, 500KHZ, 4 D/A	494F:C058
mPCIe-AIO12-16	mPCIe, A/D 12-bit, 250KHz, 4 D/A	494F:C059
mPCIe-AIO12-16E	mPCIe, A/D 12-bit, 100KHz, 4 D/A	494F:C05A
mPCIe-AI12-16A	mPCIe, A/D 12-bit, 500KHZ	494F:C058
mPCIe-AI12-16	mPCIe, A/D 12-bit, 250KHz	494F:C059
mPCIe-AI12-16E	mPCIe, A/D 12-bit, 100KHz	494F:C05A

These models are full-length "F1" mPCIe devices (30 × 50.95 mm). All units are RoHS compliant.

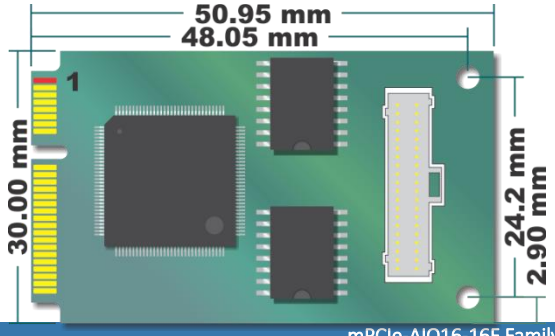
INCLUDED IN YOUR PACKAGE

mPCIe-AIO card

Available accessories include:	
CAB-mPCIe-AIO	9 inch panel-mount DB37M twisted pair cable assembly
ADAP37F-MINI	Direct plug-on terminal board mates with DB37M on CAB-mPCIe-AIO
LF-BRK-P9259-37	Mounting bracket for DB37M on CAB-mPCIe-AIO
mPCIe-HDW-KIT2	Mounting hardware for 2mm
mPCIe-HDW-KIT2.5	Mounting hardware for 2.5mm

Contact the factory for information regarding additional accessories, options, and specials that may be available to best fit your specific application requirements, such as Industrial Temperature (-40°C to 85°C).

Chapter 4: Configuration Settings



All configuration of this device is performed through software; there are no jumpers or switches to set.

Chapter 5: PC Interface

This product interfaces with a PC using a PCI Express Mini Card (mPCIe) connection; a small-form-factor, high-performance, rugged peripheral interconnect technology first introduced for use in laptops and other portable computers.

mPCIe's small size and powerful performance, combined with perfect software compatibility with PCI and PCIe peripheral designs, have led to its recent adoption as a go-to standard for embedded Data Acquisition and Control, and many other applications.

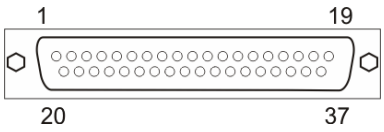
Although mPCIe is a broadly-adopted industry standard, the actual connection to the computer shares a specification with mSATA: both mSATA and mPCIe use the same edge-connector. In fact, well-designed PCs can automatically detect and configure their onboard connectors to work with either mPCIe or mSATA devices – and, according to the standards for mPCIe and mSATA they are *supposed* to do so! However, some PC manufacturers ship computers that *only* support mSATA devices. Please confirm in your PC documentation that your edge-connector is *actually* PCI Express Mini Card compliant before installing this, or any, mPCIe card. Damage might occur if you install an mPCIe device into a computer that only supports mSATA.

mPCIe defines mounting holes for securing the otherwise loose end of the card, so it is impossible for these cards to wiggle or flap themselves loose (which was a recurring problem with the older PCI Mini devices). Eliminating this concern for PCI Express Mini Cards is a major reason this standard has seen rapid adoption by the Data Acquisition and Control industry. Unfortunately, a variety of mounting standoff lengths exist; ACCES offers stand-off kits in both 2mm and 2.5mm sizes. Some computers may provide stand-offs. Please consult your computer manufacturer if it requires a different size.

The mPCIe standard, like its PCI Mini Card predecessor, was designed assuming use primarily in Laptop or Notebook and similar devices, where physical dimension is often the paramount design constraint. In Data Acquisition and Control applications low-weight and vibration tolerance tend to be of more concern.

Chapter 6: I/O Interface

Most customers will use the optional cable assembly CAB-mPCIe-AIOs D-Sub Miniature 37-pin Male connector.



For Singled-Ended analog inputs connect GND to ADC COMMON.

CAB-mPCIe-DB37M Male 37-Pin Pinout			
S.E. Signal (Diff)	Pin		Assignment
GND	1	20	GND
COMMON 0-7	2	21	ADC Ch 0 (Ch 0+)
ADC Ch 1 (Ch 0-)	3	22	ADC Ch 2 (Ch 2+)
ADC Ch 3 (Ch 2-)	4	23	ADC Ch 4 (Ch 4+)
ADC Ch 5 (Ch 4-)	5	24	ADC Ch 6 (Ch 6+)
ADC Ch 7 (Ch 6-)	6	25	GND
GND	7	26	DAC0
DAC1	8	27	DAC2
DAC3	9	28	GND
COMMON 8-15	10	29	ADC Ch 8 (Ch 8+)
ADC Ch 9 (Ch 8-)	11	30	ADC Ch 10 (Ch 10+)
ADC Ch 11 (Ch 10-)	12	31	ADC Ch 12 (Ch 12+)
ADC Ch 13 (Ch 12-)	13	32	ADC Ch 14 (Ch 14+)
ADC Ch 15 (Ch 14-)	14	33	GND
GND	15	34	GND
GND	16	35	GND
GND	17	36	GND
DIO1	18	37	DIO0
Digital GND	19		
Pin's 1 through 9 connect to ADC Sequencer #0 Pin's 11 through 19 connect to ADC Sequencer #1			

For customers needing deeper integration the on-card connector is a 40-pin latching Molex 501190-4017 connector. The mating connector is the Molex 501189-4010.

40-Pin latching wire-to-board connector			
S.E. Signal (Diff)	Pin		Assignment
ADC Ch 0 (Ch 0+)	1	2	DIO 0
ADC Ch 1 (Ch 0-)	3	4	DIO 1
ADC Ch 2 (Ch 2+)	5	6	GND
ADC Ch 3 (Ch 2-)	7	8	GND
ADC Ch 4 (Ch 4+)	9	10	GND
ADC Ch 5 (Ch 4-)	11	12	GND
ADC Ch 6 (Ch 6+)	13	14	Digital GND
ADC Ch 7 (Ch 6-)	15	16	GND
COMMON 0-7	17	18	GND
GND	19	20	GND
GND	21	22	GND
ADC Ch 8 (Ch 8+)	23	24	DAC 0
ADC Ch 9 (Ch 8-)	25	26	DAC 1
ADC Ch 10 (Ch 10+)	27	28	DAC 2
ADC Ch 11 (Ch 10-)	29	30	DAC 3
ADC Ch 12 (Ch 12+)	31	32	GND
ADC Ch 13 (Ch 12-)	33	34	GND
ADC Ch 14 (Ch 14+)	35	36	GND
ADC Ch 15 (Ch 14-)	37	38	GND
COMMON 8-15	39	40	Digital GND

Alternately, custom hardware cables and/or interfaces can be produced to fit your specific application requirement.

Register Overview

Register Offset [hex]	Read /Write	Register Name	Register Description Note: All registers 4-68 must be accessed as 32-bits. Only +0 and +1 are 8-bits
+0	RW	Reset	Board and Feature Reset command
+1	W/R	IRQ Enable / Status	IRQ Latch Clear bits and IRQ Enable Control bits / IRQ Latch Status and IRQ Enable Status
+4	W	DAC Control	DAC (LTC1664) Command Register bits
+C	R	ADC Base Clock	Frequency of the ADC Sequencer Base Clock (Hz) used to calculate the ADC Rate Divisor for desired conversion rates
+10	W/R	ADC Rate Divisor	ADC Conversion Rate = ADC Base Clock / ADC Rate Divisor (this register)
+14	W/R	ADC Rate Divisor #2	Reserved
+18	W/R	ADC ADV Sequence Gain	Each nybble controls the gain code (input range) of the respective ADC channel (0-7)
+1C	W/R	ADC ADV Sequence Gain #2	Each nybble controls the gain code (input range) of the respective ADC channel (8-15)
+20	W/R	ADC FAF Threshold	ADC FIFO Almost Full Threshold, can be enabled to generate IRQs when the threshold amount of ADC data is available in the FIFO
+28	R	ADC FIFO Count	ADC FIFO Depth: read to determine how much data is available in the FIFO
+30	R	ADC FIFO Data	ADC FIFO
+38	W/R	ADC Control	ADAS3022 and ADC Control bits
+44	W/R	DIO Data	2-bits of DIO Data
+48	W/R	DIO Control	Digital Secondary Function enable bits and direction control for each I/O Group (DIO 1 and DIO 0)
+68	R	Revision	FPGA code revision

All these registers can be operated from any operating system using any programming language, using either no driver at all (kernel mode, Linux ioperm(3), DOS, etc.) or using one of the ACCES provided drivers (AIOWDM [for Windows], APCI [for Linux & OSX]), or using any 3rd party APIs such as provided with Real-Time OSes. Addresses not explicitly documented are reserved and should not be accessed.

REGISTER DETAILS

Register bits labeled UNUSED or RSV are reserved and should be cleared to zero in all write operations and ignored in all read operations.

Reset, Offset +0 of 32-bit Memory BAR[1] Write-Only 8-bits only								
bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RESET							

Write the byte 0xFF to +0 to reset the board to the power-up state.

IRQ Enable/Clear and Status, Offset +1 of 32-bit Memory BAR[1]Read/Write *PRELIMINARY*																			
bit	D31	D30 … D24	D23	D22	D21	D20	D19	D18	D17	D16	D15 … D8	D7	D6	D5	D4	D3	D2	D1	D0
Name																			

Read IRQ Status to determine which/if any IRQs have fired (D23…D16) and which IRQs are enabled (D7…D0):

WDG: If WDG is SET then the Watchdog Timer has Barked (timed out). Refer to Watchdog Control (+4C) for details on using the Watchdog Timer feature.

EXT: If EXT is SET then an IRQ has been fired from the DIO13 Secondary Function "External IRQ". Refer to DIO Control (+48) for details on DIO Secondary Functions.

LDAC: If LDAC is SET then an IRQ has been fired from the DIO12 Secondary Function "LDAC". Refer to DIO Control (+48) for details on DIO Secondary Functions.

FOF: If FOF is SET then an IRQ has been fired because the ADC FIFO has Overrun: More data was acquired than fit in the ADC FIFO.

FAF: If FAF is SET then an IRQ has been fired because the ADC FIFO Count (+28) has reached the configured FIFO Almost Full IRQ Threshold (+20).

DTO: If DTO is SET then a DMA Timeout IRQ has been fired.

DDONE: If DDONE is SET then a DMA Done IRQ has been fired.

ADCSTART: If ADCSTART is SET then an IRQ has been fired from the DIO14 Secondary Function "ADCSTART". Refer to DIO Control (+48) for details on DIO Secondary Functions.

ADCTRIG: If ADCTRIG is SET then an IRQ has been fired from the DIO15 Secondary Function "ADCTRIG". Refer to DIO Control (+48) for details on DIO Secondary Functions.

Bits D7 through D0 indicate if the corresponding IRQ has been enabled.

Write IRQ Status bits SET to clear the latched IRQ Status bit(s). Typically, code will read +40 and write the value to +40 to clear all detected IRQs and leave the IRQ enables unchanged.

Write IRQ Enable bits SET to enable corresponding IRQ sources.

DAC Control, Offset +4 of 32-bit Memory BAR[1]Read/Write 32-bits only

bit	D31 through D24	D23 through D20				D19 through D16				D15 through D0
Name	UNUSED	C3	C2	C1	C0	A3	A2	A1	A0	16-bit DAC Counts (0-FFFF)

Please refer to the LTC1664 Data Sheet for details.

Consult the AIOAIO Software Reference, or our sample programs' source, to avoid the hassle:

DAC_SetRange1(iBoard, iChannel, iRange);

DAC_OutputV(iBoard, iChannel, double Voltage);

ADC Base Clock, Offset +C of 32-bit Memory BAR[1]Read Only 32-bits only

ADC Base Clock: Reading this 32-bit register returns the speed (in Hertz) of the clock used to generate ADC Start Conversions. Typical value is 125Million (125MHz), but for broadest compatibility software should always read this register during init, and always use the read value when calculating what, if any, divisor to write to the ADC Rate Divisor register.

ADC Rate Divisor, Offset +10 of 32-bit Memory BAR[1]Read/Write 32-bits only

ADC Rate Divisor: Write a 32-bit divisor to the ADC Rate Divisor register to control the speed at which ADC Conversions occur in selected ADC Conversion Start Modes.

Actual ADC Start Rate (Hz) = ADC Base Clock ÷ ADC Rate Divisor

ADC Rate Divisor = integer(ADC Base Clock ÷ Target ADC Start Rate)

ADC Advanced Sequencer Gain Control, Offset +18 of 32-bit Memory BAR[1]Read/Write 32-bits only

bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RSV	AIN 7 GAIN2:0			RSV	AIN 6 GAIN2:0			RSV	AIN 5 GAIN2:0			RSV	AIN 4 GAIN2:0			RSV	AIN 3 GAIN2:0			RSV	AIN 2 GAIN2:0			RSV	AIN 1 GAIN2:0			RSV	AIN 0 GAIN2:0		

Each nybble configures the gain of the corresponding Analog Input channel ONLY when the ADC is running in Advanced Sequenced mode.

Table 1 - Gain Codes

GAIN2:0 "gain code"	D2	D1	D0	Range Volts *per pin*	Range V p-p, MAX	µV/Count	Differential rejection V	Notes
0	0	0	0	±12	49.15	750		The voltage range is shown as recommended max voltage per input pin. The recommendation is slightly narrower than max to allow calibration. The voltages that can be *measured,* between the + input and the – or COMMON inputs, are double: the ±12V range will return voltages between +24V and -24V, or "48V p-p".
1	0	0	1	±5	20.48	312.5	±5.12	
2	0	1	0	±2.5	10.24	156.3	±7.68	
3	0	1	1	±1.25	5.12	75.13	±8.96	
4	1	0	0	±0.625	2.56	39.06	±9.60	
5	1	0	1	±0.3125	1.28	19.53	±9.92	
7	1	1	1	±10	40.96	625		

Gain code 6 (110) is reserved and will result in undefined behavior

ADC Advanced Sequencer Gain Control #2, Offset +1C of 32-bit Memory BAR[1]Read/Write 32-bits only

bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Name	RSV	AIN 15 GAIN2:0			RSV	AIN 14 GAIN2:0			RSV	AIN 13 GAIN2:0			RSV	AIN 12 GAIN2:0			RSV	AIN 11 GAIN2:0			RSV	AIN 10 GAIN2:0			RSV	AIN 9 GAIN2:0			RSV	AIN 8 GAIN2:0		

Each nybble configures the gain of the corresponding Analog Input channel ONLY when the ADC is running in Advanced Sequenced mode.

ADC FIFO Almost Full IRQ Threshold, Offset +20 of 32-bit Memory BAR[1]Read/Write 32-bits only

bit	D31 through D12	D11 through D0
Name	UNUSED	FAF

FAF: Write any 12-bit value (0..4095) to set the amount of entries in the ADC FIFO allowed to accumulate before a FIFO Almost Full IRQ is fired.
In Software ADC Start mode (ADC Rate Divisor (+10) cleared to zero) the FIFO is 32-bits wide, able to hold up to 4095 conversion results (+statuses).
In all other ADC Start Modes the ADC FIFO is 64-bits wide, holds two ADC Conversions (+statuses) per FIFO entry and the FIFO thus holds 8190 conversion/status pairs. Refer to the ADC FIFO (+30) register description for more details.

ADC FIFO Count, Offset +28 of 32-bit Memory BAR[1]Read-Only 32-bits only

bit	D31 through D12	D11 through D0
Name	UNUSED	FIFO Count

FIFO Count: Read FIFO Count to determine how many entries the ADC FIFO contains.
In Software ADC Start Mode (ADC Rate Divisor (+10) cleared to zero) the FIFO Count determines how many ADC Conversions (+statuses) are held in the FIFO. Read the ADC FIFO this many times to gather the acquired ADC Data.
In all other modes the FIFO Count reports the number of *pairs* of ADC Conversions are available in the FIFO. Were you to read the data from the ADC FIFO (+30) you would read two 32-bit values per FIFO Count to gather the acquired data. However, in these modes it is generally best to let DMA transfer the FIFO data, which is performed at the native 64-bit FIFO width.

ADC FIFO Data, Offset +30 of 32-bit Memory BAR[1]Read-Only 32-bits only

bit	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22 through D20	D19	D18 through D16	D15 through D0
Name	INVALID=1	RUNNING	UNUSED										
	0 ("VALID")	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	Channel2:0	RSV	Gain2:0	ADC Counts (Two's complement)

ADC FIFO Data: Read the RAW-format ADC Conversion results (in twos-complement 16-bit form) and the associated status word.

INVALID: If INVALID is SET then all other bits are undefined, and the entry should be discarded. This can occur if you read from the ADC FIFO while the ADC FIFO Count (+28) is zero.

RUNNING: SET indicates the ADC Sequencer is operating, taking either periodic (timer-driven) conversions or via the external ADC Start secondary digital function.

Channel2:0: The 3 Channel bits indicate from which Analog Input the paired ADC Counts were sampled. Refer to ADC Control (+38) for important information about the Channel bits re Differential operation.

Diff: SET indicates the paired ADC Counts were sampled in Differential mode. Refer to ADC Control (+38) for important information about the Channel bits re Differential operation.

Gain2:0: The 3 Gain bits indicate at what gain code the paired ADC Counts were sampled. Refer to the gain code table in ADC Advanced Sequencer Gain Control (+18) for how to interpret the Gain bits.

ADC Counts: 16-bit two's complement ADC counts, the ADC conversion result from the samples Channel at the specified Gain, sampled in Differential or Singled-ended / Pseudo-Differential mode as indicated by the Diff bit (D19).

Please refer to the "Software Tips" section for details on how to translate RAW-format ADC data into Volts — or skip the hassle and use our AIOAIO.dll API Library:

ADC_GetImmediateV(iBoard, pVolts, iChannel, iRange);, ADC_GetImmediateScanV(iBoard, pVolts[]); etc.

ADC Control, Offset +38 of 32-bit Memory BAR[1]Read/Write 32-bits only																
bit	D31 through D19	D18	D17	D16	D15	D14 through D12	D11	D10	D9 through D7	D6	D5	D4	D3	D2	D1	D0
Name	UNUSED	RSV	CONFIG	GO	RSV	IN*x*2:0	COM	RSV	Gain2:0	/MUX	SEQ1	SEQ0	/TEMP	RSV	CMS	RSV

Controls ADAS #0, channels 0-7

ADC Control #2, Offset +3C of 32-bit Memory BAR[1]Read/Write 32-bits only																
bit	D31 through D19	D18	D17	D16	D15	D14 through D12	D11	D10	D9 through D7	D6	D5	D4	D3	D2	D1	D0
Name	UNUSED	RSV	CONFIG	GO	RSV	IN*x*2:0	COM	RSV	Gain2:0	/MUX	SEQ1	SEQ0	/TEMP	RSV	CMS	RSV

Controls ADAS #1, channels 8-15

DIO Data, Offset +44 of 32-bit Memory BAR[1]Read/Write 32-bits only			
bit	D31 through D2	D1	D0
Name	UNUSED	DIO1	DIO0

Read DIO Data to read the digital input pins or to readback the last commanded digital output state.

Write to DIO Data to configure the digital pin(s)' high/low state for those bits in I/O Groups configured as Outputs. SET bits will output high voltage, CLEAR bits will output GND.

Refer to DIO Control (+48) for how to configure the input vs output direction of each I/O Group.

DIO Control, Offset +48 of 32-bit Memory BAR[1]Read/Write 32-bits only											
bit	D31…D25	D24	D23	D22	D21	D20	D19	D18	D17through D2	D1	D0
Name	UNUSED	RSV	edgeEXT	enEXT	RSV	RSV	edgeSTART	enSTART	UNUSED	I/O Group 1	I/O Group 0

Write DIO Control to enable Digital Secondary Functions, and to control the input vs output direction of each Digital I/O Group.

enEXT: SET enEXT to enable the "External IRQ" Digital Input Secondary Function on DIO 13 so the selected edge on the input will (optionally) generate IRQs.

enSTART: SET enSTART to enable the "ADC Start Conversion" Digital Input Secondary Function on DIO 14 so the selected edge will cause an ADC Start Event and optionally generate an IRQ.

Each Digital Input Secondary function has a configurable active edge, rising or falling. SET the corresponding edge*XXX* bit to select rising edge, CLEAR the bit for falling edge.

I/O Group1:0 SET each bit to configure the digital I/O bit in the associated I/O Group for use as digital outputs. CLEAR a bit to configure the I/O Group for use as inputs.

(D0 is I/O Group 0 which controls the output vs input direction of DIO 0; D1 is I/O Group 1 which controls the direction of DIO1)

In Windows[1], please consult the various samples (C#, Delphi, and more) to explore how to program the device. The AIOAIO Software Reference Manual.pdf provides reference material covering all AIOAIO Library APIs. A quick reference of the most-applicable functions is provided, below:

Under certain circumstances the following information might prove useful:

PCI Express Mini Card Plug-and-Play Data	
BAR[n]	Description
1:0	DMA Registers
3:2	I/O Registers

A NOTE ABOUT PERFORMANCE

The PCI Express bus and the PCI Express Mini Card standard are capable of very high bandwidth, but the latency per-transaction is roughly the same as all the other busses – it hasn't improved in decades. This means you can expect to usually see a not-less-than 1MHz transaction rate. Typical rates exceed 3MHz [0.3µs].

Unfortunately, modern Operating Systems have introduced a new source of latency, the kernel / userland division. Application code runs in userland, which must transition to the kernel in order to perform any hardware operation. This transition adds quite a lot of latency, which varies between different OSes, motherboards and revisions thereof, etcetera. A Windows XP system can see an additional 7µs per transaction; a modern computer might see 3µs or less. Any transaction from the kernel itself, however, avoids this additional overhead.

Real-time operating systems will enable the highest transaction rates possible, all the way up to the hardware limits.

The latest information can always be found on the product page on the website. Here are some useful links:

Links to useful downloads	
ACCES web site	http://acces.io
Product web page	acces.io/mPCIe-DIO-24S
This manual	acces.io/MANUALS/mPCIe-DIO-24S.pdf
Install Package	acces.io/files/packages/mPCIe-DIO-24S Install.exe
Linux / OSX	github.com/accesio/AIOComedi

[1] *In Linux or OSX please refer to the documentation at* github.com/accesio/apci.

Chapter 8: Specifications

PC Interface

PCI Express Mini Card	Type F1 "Full Length"

Analog Inputs

ADC Type	Successive approximation
Resolution	16-bit differential bipolar ADC 14 ENOB in single-ended unipolar
Sampling rate	2 Msps aggregate (1MHz per simultaneous ADC)
Number of channels	16+0, 8+4, or 0+8 (SINGLE-ENDED + DIFFERENTIAL) (software selectable)
Differential Bipolar Ranges (V)	±24.756, ±20.48, ±10.24, ±5.12, ±2.56, ±1.28, ±0.64V with 0, 0, ±5.12, ±7.68, ±8.96, ±9.60, ±9.92V common mode rejection, respectively
Single Ended Bipolar Ranges (V)	½ each differential range at 15 ENOB
4-20mA or 10-50mA	Factory options
Accuracy	0.094% Full-Scale (FS) Uncalibrated 0.0015% Calibrated[1] [1]*For best accuracy, system calibration recommended*
Int Nonlinearity Error	±0.6 LSB
No Missing Codes	16 bits
Input Impedance	>500MΩ
A/D Start Sources	Software Start, Timer Start
A/D Start Types	Single Channel or Scan
Overvoltage Protection	Current limiting through 2000Ω
Crosstalk	-120dB @ 10kHz

Analog Outputs

Number	4
Type:	Single-ended
Resolution:	16-bit
Bipolar Ranges:	±2.5V, ±5V, ±10V
Unipolar Ranges:	0-5V, 0-10V
Settling Time	20us typical, +/-10V (+/-1LSB at 16 bits)
Output Current	≥ ±10mA per channel

Environmental

Temperature	Operating	0°C to +70°C -40°C to +85°C (-T option)
	Storage	-40°C to +105°C
Humidity		5% to 95% RH, non-condensing
Dimensions	Length	50.95mm (2.006")
	Width	30.00mm (1.181")

Power

Power required	+3.3VDC @ 530mA (from mPCIe Bus)

I/O Interface Connectors

On card	Molex 501190-4017 40-pin latching
Mating	Molex 501189-4010
On-cable	Male, D-Sub Miniature, 37-pin
Mating	Female, D-Sub Miniature, 37-pin

Model Options

-T	Extended Temperature Operation (-40° to +85°C)
-I	4-20mA inputs
-PD	Pseudo-differential inputs
-Sxx	Special configurations (10-50mA inputs, input voltage dividers, conformal coating, etc.)

Chapter 9: Certifications

CE & FCC

These devices are designed to meet all applicable EM interference and emission standards. However, as they are intended for use installed on motherboards, and inside the chassis of industrial PCs, important care in the selection of PC and chassis is important to achieve compliance for the computer as a whole.

UL & TUV

Neither DC voltages above 3.3V, nor AC voltages of any kind, are consumed or produced during normal operation of this device. This product is therefore exempt from any related safety standards. Use it with confidence!

RoHS / Lead-Free Statement

All models are produced in compliance with RoHS and various other lead-free initiatives.

WARNING

A SINGLE STATIC DISCHARGE CAN DAMAGE YOUR CARD AND CAUSE PREMATURE FAILURE! PLEASE FOLLOW ALL REASONABLE PRECAUTIONS TO PREVENT A STATIC DISCHARGE SUCH AS GROUNDING YOURSELF BY TOUCHING ANY GROUNDED SURFACE PRIOR TO TOUCHING THE CARD.

ALWAYS CONNECT AND DISCONNECT YOUR FIELD CABLING WITH THE COMPUTER POWER OFF. ALWAYS TURN COMPUTER POWER OFF BEFORE INSTALLING A CARD. CONNECTING AND DISCONNECTING CABLES, OR INSTALLING CARDS, INTO A SYSTEM WITH THE COMPUTER OR FIELD POWER ON MAY CAUSE DAMAGE TO THE I/O CARD AND WILL VOID ALL WARRANTIES, IMPLIED OR EXPRESSED.

WARRANTY

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations:

GENERAL

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arriving from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to ACCES equipment not approved in writing by ACCES or, if in ACCES opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.

TERMS AND CONDITIONS

If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

COVERAGE

FIRST THREE YEARS: Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment.

FOLLOWING YEARS: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

EQUIPMENT NOT MANUFACTURED BY ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

DISCLAIMER

The information in this document is provided for reference only. ACCES does not assume any liability arising out of the application or use of the information or products described herein. This document may contain or reference information and products protected by copyrights or patents and does not convey any license under the patent rights of ACCES, nor the rights of others.

PCI EXPRESS MINI CARD STANDARD NOTICE AND EXCEPTION

The mPCI-DIO-24S family of devices are fully compliant with PCI Express Mini Card v1.2.