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PROTOTYPE CARD

MODEL PROT-DAT

USER MANUAL

file: MPROT.C1b

NOTICES

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INSTALLATION

Before installing this card carefully read the Address Selection and Option Selection sections of this manual and configure the card according to your requirements. Be especially careful with address selection. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior.

To install the card:

1. Remove power from the computer.

2. Remove the computer cover.

3. Remove the blank I/O backplate if you are going to make I/O connections to this prototype card.

4. Select the base address of the card. (See Address Selection section of this manual.)

5. Install jumpers for selection as either an I/O card or as a Memory card. (See Option Selection section of this manual.)

6. Install the card in an expansion slot. *Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.*

7. Inspect for proper fit of the card and cables and tighten screws.

8. Replace the computer cover.

If you are going to make I/O connections to this card, proper EMI cabling techniques (cable connect to chassis ground at the I/O connector, twisted-pair wiring, and, in extreme cases, ferrite level EMI protection) must be used for input/output wiring.

FUNCTIONAL DESCRIPTION

Prototype card PROT-DAT provides means for development of custom cards for use in IBM PC/XT and PC/AT or compatible computers. The card buffers all address lines, data lines, and some of the control signals. It also provides address decoding for I/O addresses 000 through 3FF hex and for memory addresses 00000 through FF000 and, allows setup of the selected address block size.

The PROT-DAT card provides approximately 35 square inches of breadboard area for custom circuit development. This breadboard area contains over 2600 plated-through holes for easy component soldering. The holes are 0.035" in diameter with 0.100" spacing. The breadboard area is surrounded by heavy buses for ground and +5VDC power.

The card is supplied with a 37-pin sub-D right-angle connector and matching mounting bracket. The properly spaced holes at the right end of the card will accommodate either one 37-pin sub-D connector, or one 25-pin and one 9-pin sub-D connector, or one 40, 50, or 60 pin flat cable connector.

PC BUS PIN CONNECTIONS AND SIGNAL LIST

62-PIN CONNECTOR

Bracket End of Card

```
                    ----------
     Ground        |B1    A1| <    -IOCHCK
     Reset    <    |B2    A2| <>   SD7
      +5VDC        |B3    A3| <>   SD6
      IRQ2    >    |B4    A4| <>   SD5
      -5VDC        |B5    A5| <>   SD4
      DRQ1    >    |B6    A6| <>   SD3
      -12VDC       |B7    A7| <>   SD2
      -OWS    >    |B8    A8| <>   SD1
      +12VDC       |B9    A9| <>   SD0            C
S     Ground       |B10  A10| <    IO CH RDY      O
O     -SMEMW  <    |B11  A11| <    AEN            M
L     -SMEMR  <    |B12  A12| <>   SA19           P
D     -IOW    <    |B13  A13| <>   SA18           O
E     -IOR    <    |B14  A14| <>   SA17           N
R     -DACK3  <    |B15  A15| <>   SA16           E
      DRQ3    >    |B16  A16| <>   SA15           N
S     -DACK1  <    |B17  A17| <>   SA14           T
I     DRQ1    >    |B18  A18| <>   SA13
D   -REFRESH*<>    |B19  A19| <>   SA12           S
E     CLK     <    |B20  A20| <>   SA11           I
      IRQ7    >    |B21  A21| <>   SA10           D
      IRQ6    >    |B22  A22| <>   SA9            E
      IRQ5    >    |B23  A23| <>   SA8
      IRQ4    >    |B24  A24| <>   SA7
      IRQ3    >    |B25  A25| <>   SA6
      -DACK2  >    |B26  A26| <>   SA5
      T/C     <    |B27  A27| <>   SA4
      BALE    <    |B28  A28| <>   SA3
      +5VDC        |B29  A29| <>   SA2          * NOTE: In XT-
      OSC          |B30  A30| <>   SA1           Class machines
      Ground       |B31  A31| <>   SA0           Pin B19 is
                    ----------                   -DACK 0
```

36-PIN CONNECTOR

End Nearest to 62-Pin Connector

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                    ----------
     -MEM CS16 >   |D1   C1 |  >  SBHE
     -I/O CS16 >   |D2   C2 | <>  LA23     C
S    IRQ10     >   |D3   C3 | <>  LA22     O
O    IRQ11     >   |D4   C4 | <>  LA21     M
L    IRQ12     >   |D5   C5 | <>  LA20     P
D    IRQ15     >   |D6   C6 | <>  LA19     O
E    IRQ14     >   |D7   C7 | <>  LA18     N
R    -DACK0   <    |D8   C8 | <>  LA17     E
     DRQ0      >   |D9   C9 |  >  -MEMR    N
S    -DACK5   <    |D10  C10|  >  -MEMW    T
I    DRQ5      >   |D11  C11| <>  SD08
D    -DACK6   <    |D12  C12| <>  SD09     S
E    DRQ6      >   |D13  C13| <>  SD10     I
     -DACK7   <    |D14  C14| <>  SD11     D
     DRQ7      >   |D15  C15| <>  SD12     E
     +5VDC         |D16  C16| <>  SD13
     -MASTER       |D17  C17| <>  SD14
     Ground        |D18  C18| <>  SD15
                    ----------
```

NOTES

1. > : Symbols pointing toward the connector designate signals <u>into</u> the card from devices on the bus.

2. < : Symbols pointing away from the connector designate signals <u>from</u> the card to devices on the bus.

3. <>: Double symbols indicate bi-directional signals.

4. A "minus" sign before the signal name signifies active low.

5. In the PC and PC/XT, the bus consists only of the 62-pin portion. Some of the signal names are different but the functionality remains the same.

BUS SIGNAL LIST

The signal names used in this listing are for the AT Bus. When appropriate, the older names used for the PC/XT are included in parenthesis. "I" indicates that the signal is an input from the bus to the card and "O" signifies an output from the card to the bus. See the AT technical manual for a more detailed description of these signals.

SIGNAL	I/O	DESCRIPTION
-OWS (or -ENDXFR)	I	Zero Wait State. Fast bus devices pull this line low to prevent the CPU from inserting extra wait cycles. The OWS signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles.
AEN	O	Address Enable. When this line is high,the DMA controller has control of the address lines, data lines, memory read/write, and I/O read/write.
BALE (ALE)	O	Address Latch Enable. This line is used to latch valid addresses and memory decodes from the microprocessor. It's available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with AEN). Microprocessor addresses SA0 through SA19 are latched with the falling edge of BALE. BALE is forced high during DMA cycles.
CLK	O	System Clock. This clock signal may vary from 6 MHz to 8.33 MHz or higher.
-DACK1-7		

(-DACK0-3)	O	DMA acknowledge lines used to acknowledge DMA requests (DRQ). Active low.
DRQ0-7 (DRQ1-3)	O	DMA Request lines from devices on the bus that need DMA service. The line must be held high until the corresponding DACK line goes active (low). These lines are prioritized. DRQ0 has highest priority and DRQ7 has lowest priority. DRQ0 through DRQ3 perform 8-bit transfers and DRQ5 through DRQ7 perform 16-bit transfers. DRQ4 is not available on the I/O channel.
-I/O CH CHK	I	I/O Channel Check. When low, a device on the bus has detected a parity error.
I/O CH RDY	I	I/O Channel Ready. Pulled low (not ready) by a memory or I/O device on the bus that needs more time. Never hold low for more than 10 clock cycles (XT) or 2.5 usec (AT). Cycles are extended in integral multiples of CLK cycles.
-I/O CS16	I	I/O 16-bit Chip Select. Signals a 16-bit one-wait-state I/O cycle. This signal is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mA.
-IOR	O	I/O Read command. This line tells an I/O device on the bus to drive its data onto the data bus. Active low.

-IOW	O	I/O Write command. This line instructs an I/O device on the bus to read the data present on the data lines.
IRQ2-7, IRQ9-12, & IRQ14-15	I	Interrupt Request lines used by peripherals when they need attention. Interrupt requests are prioritized with IRQ9 through IRQ12 and IRQ14 through IRQ15 have the highest priority (IRQ9 is the highest) and IRQ2 through IRQ7 have the lowest priority (IRQ7 is the lowest). An interrupt line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine) Interrupt 8 is used for the real time clock. Interrupt 13 is not available on the I/O channel.
LA17-23	I/O	Unlatched address lines valid when BALE is high. I/O devices should latch these signals when BALE falls. Used for one-wait-state memory cycles.
-MASTER	I	A processor on the I/O channel may use this signal with a DRQ to gain control of the address, data, and control lines of the bus. The controlling processor may need to assume responsibility to refresh system memory every 15 usec.
-MEM CS16	I	Memory 16-Bit Chip Select signals a 16-bit, one-wait-state memory cycle. This signal is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mA.

-MEMR	O	Memory Read (AT). This signal tells bus memory devices to put data onto the data bus. See -SMEMR to follow.
-MEMW	O	Memory Write (AT). This signal tells bus memory devices to put the data onto the data bus. See -SMEMW to follow.
OSC	O	A 50% duty cycle clock signal with a frequency of 14.31818 MHz
-REFRESH	O	This line is used in the AT to signal a memory refresh cycle. -DACK0 is used for this purpose in the PC/XT. Active low.
RESET DRV	O	Used to reset or initialize sys tem logic on power-up or during low line voltage. Synchronized to the falling edge of CLK.
SA0-19 (A0-19)	O	Address lines for the first 1 MB of memory. SA0 is the least significant bit (LSB).
SBHE	O	Bus High Enable (system) indi cates a 16-bit transfer of data.
SD0-15	I/O	Data bits. SD0 is the least significant bit (LSB).
-SMEMR	O	Memory Read. This command tells memory on the bus to drive its data onto the data bus. Used only with the lower 1 MB of memory. Active low.
-SMEMW	O	Memory Write. This command in structs memory devices on the bus to store the data present on the data bus. Used only on the lower 1 MB of memory. Active low.
T/C	O	Terminal Count. This signal provides a pulse when the termi

nal count for a DMA cycle is reached.

I/O ADDRESS MAP

The PROT-DAT card address can be selected anywhere within the I/O address range 000-3FF hex or the Memory address range 00000-FF000 providing that the address does not overlap that of other installed functions. It is intended that I/O base addresses be selected at four-byte intervals and that memory base address be selected at 4096 byte intervals.

Table 1 lists standard I/O address assignments.

TABLE 1.

Hex Range	Usage
000-00F	DMA Chip 8237A-5
020-021	Interrupt 8259A
040-043	Timer 8253-5
060-063	PPI 8255A-5
080-083	DMA Page Register
0AX	NMI Mask Register
0CX	Reserved
0EX	Reserved
100-1FF	Not Usable
200-20F	Game Control
210-217	Expansion Unit
220-24F	Reserved
278-27F	Reserved
2F0-2F7	Reserved
2F8-2FF	Asynchronous Comm. (Secondary)
300-31F	Prototype Card
320-32F	Fixed Disk
378-37F	Printer
380-38C**	SDLC Communications
380-389**	Binary Synchronous Comm.(Secondary)
3A0-3A9	Binary Synchronous Comm.(Primary)
3B0-3BF	IBM Monochrome Display/Printer
3C0-3CF	Reserved
3D0-3DF	Color/Graphics
3E0-3E7	Reserved
3F0-3F7	Diskette
3F8-3FF	Asynchronous Comm. (Primary

** These options can not be used together - addresses overlap

STANDARD ADDRESS ASSIGNMENTS FOR 286/386/486 COMPUTERS

Hex Range	Usage
000-01F	DMA Controller 1
020-03F	INT Controller 1, Master
040-05F	Timer
060-06F	8042 (Keyboard)
070-07F	Real Time Clock, NMI Mask
080-09F	DMA Page Register
0A0-0BF	INT Controller 2
0C0-0DF	DMA Controller 2
0F0	Clear Math Coprocessor Busy
0F1	Reset Coprocessor
0F8-0FF	Arithmetic Processor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Asynchronous Comm'n (Secondary)
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC or Binary Synchronous Comm'n 2
3A0-3AF	Binary Synchronous Comm'n 1
3B0-3BF	Monochrome Display/Printer
3C0-3CE	Local Area Network
3D0-3DF	Color/Graphic Monitor
3F0-3F7	Floppy Diskette Controller
3F8-3FF	Asynchronous Comm'n (Primary)

ADDRESS SELECTION

The PROT-DAT card address is set by DIP switch SW1. That switch controls I/O address bits A2 through A9 if jumpers are installed in the upper positions at W1, W2, W3, W4, W5, W6, W7, and W8. If those jumpers are installed in the lower positions at those locations, then the DIP switch controls memory address bits A12 through A19.

In order to set the base address, first convert the desired hex address to binary form. Then, *for each "1" of the binary address, set the corresponding DIP switch to OFF and for each "0" of the binary number, set the corresponding DIP switch to ON.*

For example, to program a base address of hex 300 (11000000 binary) set switches A9 and A8 to the OFF position and switches A7 through A2 to the ON position.

NOTE

Carefully review the Address Selection reference table on the previous page before selecting the card address. If the address of two installed functions overlap, you will experience unpredictable computer behavior.

OPTION SELECTION

You can use the card as an I/O card or as a Memory card. Also, you can select the size of a block of addresses reserved for this card. Base Address is set by DIP switches as described in the previous section.

I/O Card or Memory Card

If the card will be used as an I/O card, place the jumper between the leftmost pins at the location labeled I/O MEM. If the card is going to be used as a memory card, place that jumper between the rightmost pins.

Jumpers W1, W2, W3, W4, W5, W6, W7, and W8 select either address lines A2 through A9 (if to be an I/O card) or address lines A12 through A19 (if to be a memory card) as input for the address decoding circuit. If the eight jumpers are installed between the upper two pins at each position, then I/O card addresses A2 through A9 are selected. If the jumpers are installed between the lower two pins, then Memory addresses A12 through A19 are activated.

Block of Addresses Reserved

The size of a block of addresses reserved for the PROT-DAT card is selected by the combination of DIP switch settings and jumpers marked 8, 16, 32, 32K, 64K, 128K, and 256K. The jumper positions marked 8, 16, and 32 are primarily used to set I/O address space required by the card. The remaining jumper positions are primarily used to set memory space to be occupied by the card. If no jumpers are installed, then the block size is four bytes for an I/O card and 2K bytes for a memory card. Refer to the following table:

I/O Card Address Space	Memory Card Address Space	Install Jumpers
8 Bytes	4K Bytes *	8
16 Bytes	8K Bytes *	16
32 Bytes	16K Bytes *	32
64 Bytes *	32K Bytes	32K
128 Bytes *	64K Bytes	64K
256 Bytes *	128K Bytes	128K
512 Bytes *	256K Bytes	256K

Note: Selections marked "*" are infrequently used.

Base Address Selection When Address Blocks are Reserved

As described in the previous section of this manual, DIP switches A2 through A9 are used to set the base address. The A2 position corresponds to the least significant bit of the address in hexadecimal code and the A9 position corresponds to the most significant bit. If a block size of four bytes is selected for an I/O card application (or 2K bytes for memory operation), then all eight switches are available to set the base address. If one or more block-reserving jumpers are installed, then certain DIP switches must be placed in the OFF position as follows:

8 Bytes I/O or 4KB Memory:	A2 must be OFF
16 Bytes I/O or 8KB Memory:	A2 and A3 must be OFF
32 Bytes I/O or 16KB Memory:	A2, A3, and A4 must be OFF
64 Bytes I/O or 32KB Memory:	A2, A3, A4, and A5 must be OFF
128 Bytes I/O or 64KB Memory:	A2 through A6 must be OFF
256 Bytes I/O or 128KB Memory:	A2 through A7 must be OFF
512 Bytes I/O or 256KB Memory:	A2 through A8 must be OFF

Eight or 16-bit Operation

For 16-bit operation, it is necessary to complete wiring on IC U7 and to add a 74LS125 as shown within dotted lines on the schematic. Further, you may require different or additional circuitry depending on how you wish this card to interface to the computer I/O bus.

SPECIFICATION

Computer Connector: Gold edge connector for IBM PC/XT,PC/AT, or compatible computers.

Breadboard Area: Approximately 35 square inches with 0.035" plated-through holes spaced 0.100" apart. Heavy ground and +5VDC buses surround the breadboard area.

Address Signals: Address lines are buffered by type 74LS244 line drivers, labeled, and available at assigned pads. See Schematic.

Data Signals: Data lines D0 through D15 are buffered by two type 74LS245 transceiver, and are available at assigned pads. See Schematic.

Address Decode: Decoding provided for either I/O addresses or for Memory addresses. Card address is DIP switch selectable.

Card Address Block: Jumper selectable; 8, 16, or 32 bytes for I/O card use and 32K, 64K, 128K, or 256K for Memory card use.

Output Connector: A 37-pin Sub-D right angle connector and mounting bracket are included. Properly spaced holes are provided for other combinations of connectors such as 9-pin Sub-D and 25-pin Sub-D. The card will also accept 50-pin ribbon cable connectors.

Bracket: Mounting bracket for standard 37-pin Sub-D connector included.

Card Size: Full size PC/XT card (13.25" x 3.87")

Operating Temperature: 0 to +60°C.

Storage Temperature: -20 to +85°C.

Humidity: 5% to 95% RH, non-condensing.

SCHEMATIC

WARRANTY

Prior to shipment, ACCES equipment is thoroughly inspected and tested to applicable specifications. However, should equipment failure occur, ACCES assures its customers that prompt service and support will be available. All equipment originally manufactured by ACCES which is found to be defective will be repaired or replaced subject to the following considerations.

TERMS AND CONDITIONS

If a unit is suspected of failure, contact ACCES' Customer Service department. Be prepared to give the unit model number, serial number, and a description of the failure symptom(s). We may suggest some simple tests to confirm the failure. We will assign a Return Material Authorization (RMA) number which must appear on the outer label of the return package. All units/components should be properly packed for handling and returned with freight prepaid to the ACCES designated Service Center, and will be returned to the customer's/user's site freight prepaid and invoiced.

COVERAGE

First Three Years: Returned unit/part will be repaired and/or replaced at ACCES option with no charge for labor or parts not excluded by warranty. Warranty commences with equipment shipment. Following Years: Throughout your equipment's lifetime, ACCES stands ready to provide on-site or in-plant service at reasonable rates similar to those of other manufacturers in the industry.

EQUIPMENT NOT MANUFACTURED BY ACCES

Equipment provided but not manufactured by ACCES is warranted and will be repaired according to the terms and conditions of the respective equipment manufacturer's warranty.

GENERAL

Under this Warranty, liability of ACCES is limited to replacing, repairing or issuing credit (at ACCES discretion) for any products which are proved to be defective during the warranty period. In no case is ACCES liable for consequential or special damage arising from use or misuse of our product. The customer is responsible for all charges caused by modifications or additions to ACCES equipment not approved in writing by ACCES or, if in ACCES opinion the equipment has been subjected to abnormal use. "Abnormal use" for purposes of this warranty is defined as any use to which the equipment is exposed other than that use specified or intended as evidenced by purchase or sales representation. Other than the above, no other warranty, expressed or implied, shall apply to any and all such equipment furnished or sold by ACCES.